NEW Product

DDR12

Application Note 133

ARTESYN® TECHNOLOGIES

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1. Introduction

The application note describes the features and functions of Artesyn Technologies' DDR12 series of high power density dual adjustable output DC/DC Converters. The open-frame DDR12 module is currently available in a vertical mount package and is designed for use in workstation, computing, industrial and communications applications.

2. Models

The DDR12 series comprises 1 model, as listed in Table 1 .

Model	Input Voltage	Output Voltage	Output Current
DDR12	10.8 to 13.2VDC	2.32 to 2.75V 1.160 to 2.375V	25A 8A

Table 1 - Available DDR12 Models

Features

- Tracking dual output voltages (1.25V @ 8A, 2.5V @ 25A)
- Output voltage trim
- Output voltage remote sense (V_{ddq} only)
- Sink capability for logic terminations
- Power good output signal (open collector)
- Over-voltage and over-current protection
- Remote ON/OFF

3. General Description

3.1 Electrical Description

The DDR12 is implemented using a voltage-mode controlled Buck/Boost topology. A block diagram is shown in Figure 1.

The V_{ddq} output is adjustable over a range of 2.32V - 2.75V by using an external voltage divider circuit tied to the +SENSE pin (See section 7.3). The V_{tt_ref} output is precisely regulated to 50% of V_{ddq}, with a maximum tolerance of ±1% over line, load and temperature. V_{tt} accurately tracks V_{ref} and V_{ddq}, per the tracking specifications in the datasheet.

The V_{tt} output is also capable of sinking current as required by logic terminations.

The converter can be shut down via a remote OUTEN input. The input runs with positive logic, which is compatible with standard logic devices. Positive logic implies the converter is enabled if the OUTEN pin is high (or floating) and is disabled if pulled low.

The power good signal is an open collector, which is pulled low by the PWM controller when it detects the output is not within ±10% of its value. This pin is pulled high when the output voltage is within this range.

The DDR12 module is protected from over-current and short-circuit conditions on the output. The current flow is monitored across the output inductor of both the V_{ddq} and V_{tt} channels. When the PWM detects an over-current condition the DDR12 module latches off, requiring the OUTEN pin to be cycled.

The DDR12 module is also protected from over-voltage conditions on the output. If an over-voltage condition is detected the module latches off, requiring the OUTEN pin to be cycled.

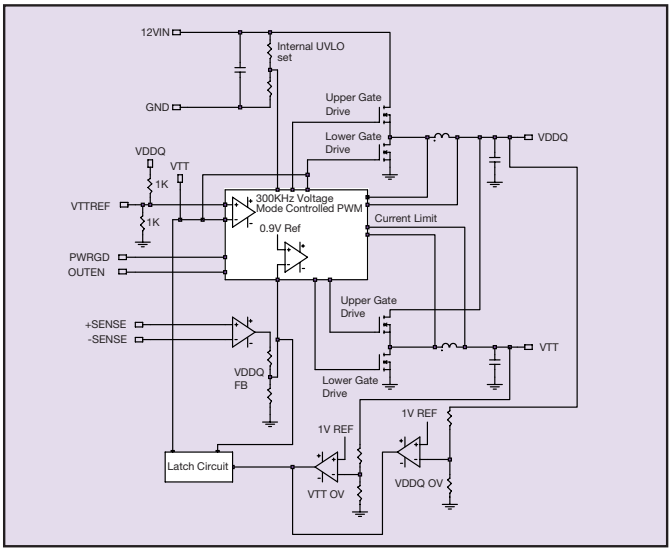

Figure 1 - Electrical Block Diagram

3.2 Physical Construction

The DDR12 is constructed using a multi-layer FR4 PCB. SMT power components are placed on one side of the PCB, and all low power control components are placed on the other side. Heat dissipation of the power components is optimized, ensuring the control components are not thermally stressed.

The converter is an open-frame product and has no case or case pin. The open-frame design has several advantages over encapsulated closed devices. Among these advantages are:

- Cost: no potting compound, case or associated process costs involved
- Thermals: the heat is removed from the heat generating components without heating more sensitive, less tolerant components
- Environmental: some encapsulates are not kind to the environment and create problems in incinerators. Further more open-frame converters are more easily re-cycled
- Reliability: open-frame modules are more reliable for a number of reasons, including improved thermal performance and reduced TXE stresses

4. Features and Functions

4.1 Wide Operating Temperature Range

The DDR12 module's ability to accommodate a wide range of ambient temperatures is the result of its extremely high power conversion efficiency and resultant low power dissipation, combined with the excellent thermal performance of the PCB substrate. The maximum output power, which the module can deliver, depends on a number of parameters, primarily:

- Input voltage range
- Output load current
- Air velocity (see de-rating curves)
- Mounting orientation of target application PCB
- Target application PCB design especially ground planes. These can be effective heat-sinks for the converter.

With 200LFM of airflow the DDR12 module can be operated to an ambient temperature of +80°C.

4.2 Output Voltage Adjustment

The output voltage set point of both V_{ddq} and V_{tt} can be trimmed externally using voltage divider networks on the +SENSE and V_{ref} pins respectively. Details on how to trim the output voltages are in Appendix 1.

4.3 Undervoltage Lockout

The DDR12 has a built in under voltage lockout to ensure reliable operation of the DDR12 module. The lockout prevents the unit from operating when the input voltage is too low. The DDR12 has an input operating range of 10.8V to 13.2V with UV lockout occurring between 9.7V to 10.4V.

4.4 Current Limit and Short-Circuit Protection

The DDR12 module has built-in latching over current and short-circuit protection on both the V_{ddq} and V_{tt} channels. The module monitors the current using the resistance of the output inductors. When an over current condition occurs on V_{ddq} the module latches off, when an over current condition occurs on V_{tt} the V_{tt} voltage folds back.

4.5 Output Over-voltage Protection

Output over-voltage conditions on V_{ddq} are monitored by a seperate feedback circuit which signals the PWM controller to turn on the lower switch and turn off the upper switch in the buck converter. If the upper switch has “failed-short”, this will have a “crowbar” effect on the input bus.

4.6 OUTEN (Remote ON/OFF)

The unit is turned on if the OUTEN pin is high (or floating). Pulling the pin low will turn off the unit. To guarantee turn-on the enable voltage must be above 2.0V and to turn off the enable voltage must be pulled below 0.8V.

Figures 2 and 3 show the response of the unit to switching on and off using the OUTEN pin.

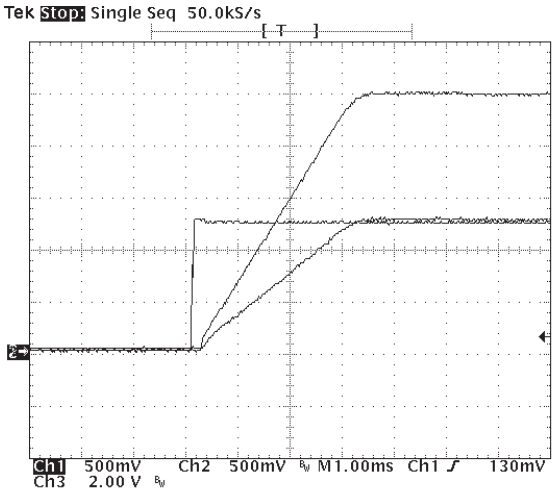

Figure 2 - Typical Response to OUTEN being enabled (Chan1: OUTEN, Chan2: V_{ddq}, Chan3: V_{tt})

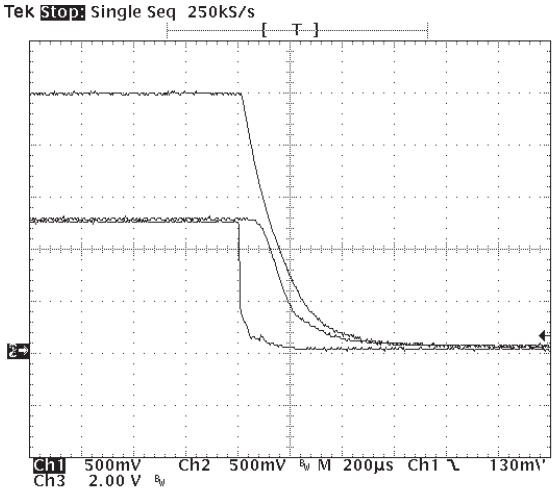

Figure 3 - Typical Response to OUTEN being disabled (Chan1: OUTEN, Chan2: V_{ddq}, Chan3: V_{tt})

4.7 Current Sinking Capabilities

The Vtt output of the DDR12 converter is able to be a current sink as well as a current source. It is able to sink or source 8A of current. V_{ddq} is only able to be a current source.

4.8 POWER GOOD Signal

The DDR12 module has a power good indicator output. This output pin uses positive logic and is open collector. When the output of the module is within ±10% of the nominal set point, the power good pin is set high. Figure 4 shows power good being pulled up by an external 3.3V supply in response to the DDR12 module being enabled.

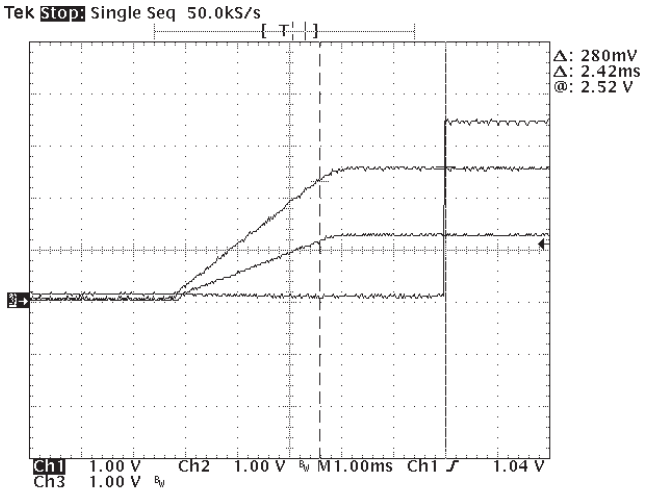

Figure 4 - Power Good Signal being pulled high by external 3.3V source

5. Safety

5.1 Input Fusing

In order to comply with safety requirements, the user must provide a fuse in the unearthed input line if an earthed input is used. The reason for putting the fuse in the unearthed line is to avoid earth being disconnected in the event of a failure. If an earthed input is not being used then the fuse may be in either input line.

6. Use in a Manufacturing Environment

6.1 Resistance to Solder Heat

The DDR12 converter is intended for PCB mounting. Artesyn Technologies has determined how well the product can resist the temperatures associated with soldering of PTH components without affecting its performance or reliability. The method used to verify this is MIL-STD-202 method 210D. Within this method two test conditions were specified; Soldering Iron condition A and Wave solder Condition C.

For the soldering iron test, the UUT was placed on a PCB with the recommended PCB layout pattern shown in section 7.1. A soldering iron set to 350°C±10°C was applied to each terminal for five seconds. The UUT was then removed from the test PCB and examined under a microscope for any reflow of the pin solder or physical change to the terminations. None was found.

For the wave solder test, the UUT was again mounted on a test PCB. The unit was wave soldered using the conditions shown in Table 2. The UUT was inspected after soldering and no physical change was found on the pin terminations.

6.2 Water Washing

Where possible, a no-clean solder paste system should be used for solder attaching the DDR12 product onto application boards. The DDR12 is suitable for water washing applications, because it does not have entrapment areas where water and residues may become trapped long term. However, the user must ensure the drying process is sufficient to remove all water from the converter after washing - never power the converter unless it is fully dried. The user's process must clean the soldered assembly in accordance with ANSI/J-STD-001.

6.3 ESD Control

DDR12 units are manufactured in an ESD controlled environment and supplied in conductive packaging to prevent ES damage occurring before or during shipping. It is essential they are unpacked and handled using approved ESD control procedures. Failure to do so could affect the lifetime of the converter.

7. Applications

7.1 PCB Layout

The pin diagrams for the DDR12 are detailed in Figure 5.

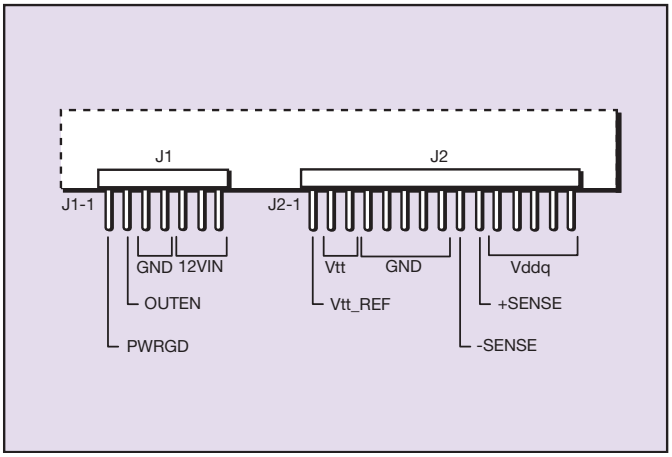

Figure 5 - Pin Diagram for the DDR12

7.2 Optimum Thermal Performance

The electrical operating conditions of the DDR12 namely:

- Input voltage, V_{in}
- Output voltages, V_{ddq}, V_{tt}
- Output current, I_{ddq}, I_{tt}

Determine how much power is dissipated within the converter. The following parameters further influence the thermal stresses experienced by the converter:

- Ambient temperature
- Air velocity
- Thermal efficiency of the end system application
- Parts mounted on system PCB that may block airflow
- Real airflow characteristics at the converter location

Figure 6 indicates the thermal reference point location on the DDR12 converter.

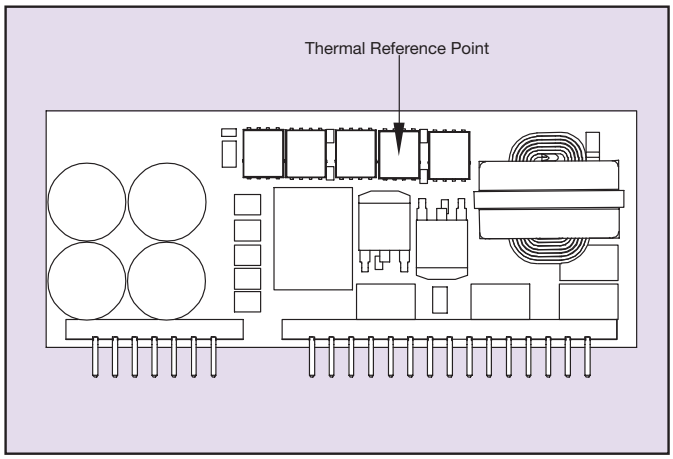

Figure 6 - Thermal Reference Point Location

In order to simplify the thermal design, a graph is provided in the data sheet and repeated in Figure 7. These derating graphs show the load current of the DDR12 versus the ambient air temperature and forced air velocity. However, since the thermal performance is heavily dependent upon the final system application, the user needs to ensure the thermal reference point temperatures are kept within the recommended temperature rating. It is recommended that the thermal reference point temperatures are measured using a thermocouple or an IR camera. In order to comply with stringent Artesyn de-rating criteria the ambient temperature should never exceed 80°C.

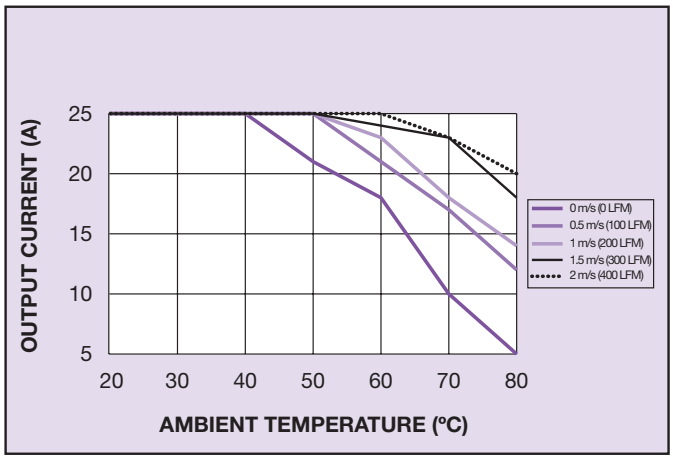

Figure 7 - Thermal De-rating Curve

7.3 Output Voltage Adjustment

The V_{ddq} output on the DDR12 is capable of being trimmed by adding an external voltage divider circuit on the +SENSE pin as seen in figure 8. Equation 1 calculates the value for R_{set} based upon a desired V_{ddq} output voltage.

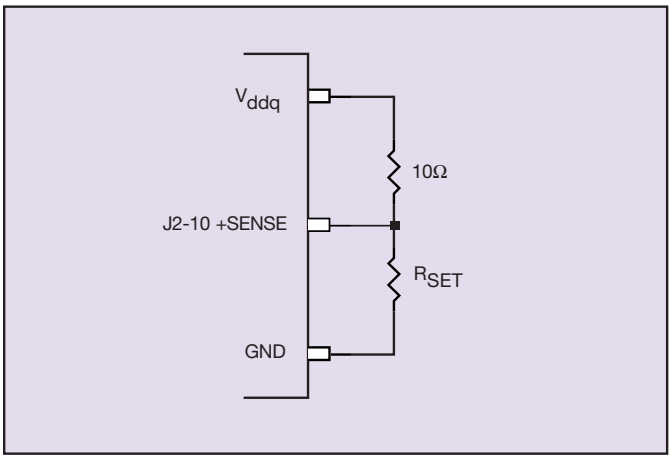

Figure 8 - Voltage Divider Network for Trimming V_{ddq} Output

$$R_{set} = (21.052/(V_{ddq} - 2.316)$$

Equation 1

Example:
V_{ddq} = 2.5V
R_{set} = 21.052 / (2.5 - 2.316)
R_{set} = 114Ω

Power loss for R_{set}:
P = 2.32^2 / R_{set}

Example:
R_{set} = 114Ω
Ploss in R_{set} = 2.32^2 / 114Ω
Ploss = 47mW

7.4 Parallel Operation

Parallel operation of multiple DDR12 VRM's is not recommended. If unavoidable, Oring diodes must be used to de-couple the outputs. It should be noted this measure would adversely affect power conversion efficiency.

7.5 Output Capacitance

When powering loads with large dynamic current requirements, improved voltage regulation can be obtained by inserting capacitors as close as possible to the load. The most effective technique is to locate low ESR ceramic capacitors as close to the load as possible, using several capacitors to lower the overall ESR. These ceramic capacitors will handle the short duration high frequency components of the dynamic current requirement. In addition, higher values of electrolytic capacitors should be used ot handle the mid-frequency components. It is recommended that you use three - 560µF OS-Con type capacitors on both the V_{ddq} and V_{tt} outputs.

It is equally important to use good design practices when configuring the DC distribution system. Low resistance and low inductance PCB layout traces should be utilized, particularly in the high current output section. Remember that the capacitance of the distribution system and the associated ESR are within the feedback loop of the power module. This can have an effect on the modules compensation capabilites and its resultant stability and dynamic response performance. With large values of capacitance, the stabilty criteria depend on the magnitude of the ESR with respect to the capacitance.

7.6 Reflected Ripple Current and Output Ripple and Noise Measurement

The measurement set-up outlined in Figure 9 has been used for measuring output ripple and noise and input ripple current measurements.

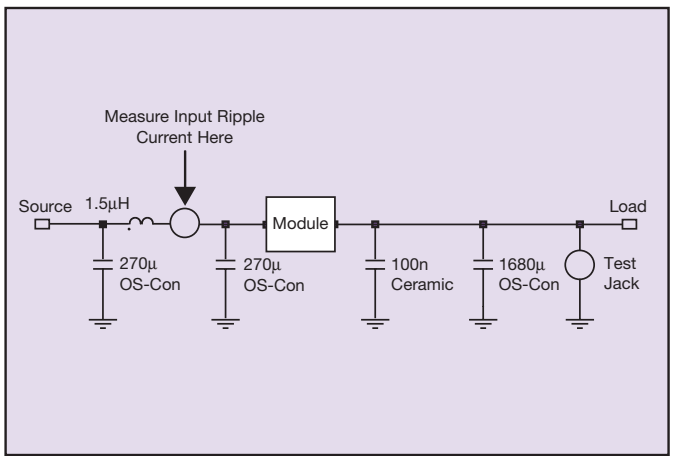

Figure 9 - Set-up for Measuring Input Ripple Current and Output Ripple Voltage