NEW Product

VRM64 SERIES

Application Note 185

ARTESYN® TECHNOLOGIES

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1. Introduction

This application note describes the features and functions of Artesyn Technologies' VRM64 series of high power density non-isolated dc-dc converters. These open-frame, single-output modules are targeted specifically at users of AMD® Opteron™ processors. The VRM64 series features extremely fast transient response to meet the dynamic current requirements of today's microprocessors and fast switching logic.

The VRM64 series operates over an input voltage range of 10.8 Vdc to 13.2 Vdc and can operate over an ambient temperature range of 0 °C to +60 °C. High efficiency operation is achieved through the use of synchronous rectification, silicon integration, and digital control techniques in conjunction with a multi-phase topology. The modules are fully protected against output overcurrent and overvoltage conditions, and input undervoltage and overvoltage. Standard features include output enable, remote sense, power good signal, voltage identification (VID control), and are fully compatible with the requirements of the AMD specification (Publication #31514 Rev 2.0)

The series has been designed primarily for computing applications and is suitable for use in systems which use the AMD® Opteron™ processors. These converters may also be used in other applications where the load requires similar voltage and current levels. Advanced technology, state-of-the-art components, conservative design practices, advanced thermal packaging and automated assembly all contribute to making the VRM64 series a highly reliable product.

2. Models

The VRM64 series comprises one model, as listed in Table 1.

Model	Input Voltage	Output Voltage	Output Current
VRM64-80-12-U	12 Vdc	0.8-1.55 V	80 A

Table 1 - Available VRM64 Models

Features

- Meets AMD requirements
- Wide operating temperature range (0 °C to +60 °C ambient)
- 5 bit VID code output voltage setting
- No minimum load requirement
- Output enable
- Differential remote sense compensation
- Constant switching frequency
- Over-current protection
- Short-circuit protection
- Output over-voltage protection signal (OVP)
- Power Good signal
- VRM present signal
- Fused input
- Input undervoltage and overvoltage protection

3. General Description

3.1 Electrical Description

A block diagram of the VRM64 converter is shown in Figure 1. They utilize a non-isolated interleaved multi-phase buck topology with 6 power conversion channels on 5 phases. This technique results in an effective output ripple frequency of over 4 MHz. The VRM64 converters operate at a typical switching frequency of 830 kHz giving an output ripple waveform of 4.2 MHz. In addition to simplifying the task of output capacitive filtering, this technique results in superior transient response to handle severe dynamic load requirements. Very high efficiency power conversion is achieved through the use of synchronous rectification techniques. The VRM needs a 5 V auxiliary supply (+5_ALWAYS) to supply the master controller and other logic circuits. This supply should by well smoothed and stabilized. The maximum load current is 250 mA.

The regulated voltage on the output pins is governed by the voltage on the module's sense pins, Vsense+ and Vsense– (COREFB L and COREFB H respectively).

The output is adjustable over a range of 0.8 V to 1.55 V by means of the 5 bit VID interface as described in sections 4.4 and 8.3. The converter may be shut down by means of an output enable signal which is compatible with standard logic devices. A power good signal is provided for verifying the operation of the converter to the user's system.

The VRM64 converters feature continuous overvoltage and cycle-by-cycle overcurrent protection with automatic recovery. In accordance with the AMD specification, the default setting is a 'trip' current limit (reset by cycling the +12 V supply. It may be reset to automatic recovery by removing R2. More fully described in Section 4.11.

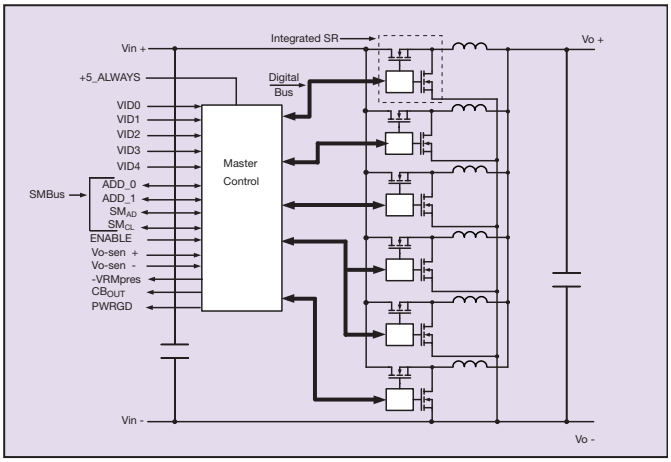

Figure 1 - Electrical Block Diagram

3.2 Physical Construction

The VRM64 converter is constructed using a multi-layer FR4 PCB. SMT components are placed on both sides of the PCB. Heat dissipation of the high power components is conducted to an included heatsink structure. The primary cooling path is via forced air convection to this heatsink.

The VRM64 converter plugs into a socket on the user's motherboard by means of a gold-plated edge connector on the converter's PCB and is oriented vertically to the motherboard. Recommended mating connectors are listed in the VRM64 datasheet.

The converter is an open-frame product with high conductivity thermal paths to the cooling environment. A separate paper discussing the benefits of open-frame DC/DC converters (Design Note 102) is available at **www.artesyn.com.**

4. Features and Functions

4.1 Operating Temperature Range
The VRM64's ability to accommodate a wide range of ambient temperatures, from 0 °C to 60 °C, is the result of its extremely high power conversion efficiency and resultant low power dissipation, combined with the excellent thermal performance of the PCB substrate and included heatsink structure. The maximum output current that the module can deliver depends on a number of parameters, but primarily the air velocity and temperature.

Thermal derating curves are shown in Figure 4 of section 8.1 to simplify the design task and allow the power system designer to determine the maximum output current at which the VRM64 module may be operated for a given ambient temperature and airflow condition. Each of the six power ICs are individually protected, and will latch off if their junction temperature is excessive. If this happens, the current limit point is reduced in proportion, so the maximum current will not be available. Reset is by recycling the +12 V. In addition, there is a central temperature protection system, operating at a nominal PCB temperature of 115 °C. This will force CB_{OUT} active high. The signal is not latched, but there is a 10 °C hysterisis. The customer is responsible to ensure sufficient force air cooling appropriate to the operating conditions. See Figure 5 for the temperature reference point.

4.2 Current Sharing
The VRM64 series of converters contains current sharing circuitry. If current sharing is required between a number of VRMs, all the I_{SHARE} pins should be connected together, and all the SGND pins should be connected together. The remote sense connections should be made to same points at the load for all VRMs. Note that I_{SHARE} uses pin 49, and this is different to the AMD pin allocation. If not used, leave pin 49 unconnected.

4.3 Transient Response
The VRM64 series is designed to power the latest AMD® Opteron™ processors that require VRMs, and others requiring similar performance from the VRM. These processor loads have extremely high current slew rates. Most of this current slew rate is handled by low ESR capacitors close to the processor. Consequently, the current slew rate will be maximum right at the processor chip die, less at the microprocessor connector, and still less at the edge connector of the VRM64 converter. The slew rates referred to in this application note and in the VRM64 datasheet are measured at the VRM's output capacitors (see recommendations). The VRM64 converter's output voltage is specified to stay within the regulation limits up to these slew rates with the recommended output capacitor configurations. This high current slew rate performance is achieved by means of a five phase topology operating at a high switching frequency.

The recommended minimum output capacitor configuration consists of 48 x 22 µF MLCC capacitors. There is no need for aluminum polymer capacitors, although they may be used if desired.

The placement and interconnection of the output capacitors is also critical. Refer to sections 8.5 and 8.8 for more information on capacitor selection, placement, interconnection, and typical converter transient response performance.

4.4 Output Voltage Adjustment (VID)
The output voltage of the VRM64 can be set between 0.8 V and 1.6 V by means of a 5 bit Voltage Identification Input (VID) code in 25 mV steps. Note that the setpoint voltage is the upper limit of the output voltage regulation window and that the actual measured output voltage will typically be lower than the setpoint voltage depending upon the converter output resistance and the load current. See section 8.3 for information on how to set the output voltage. Details of the drive requirements for this interface can be found in the VRM64 datasheet and in section 8.6 of this application note.

4.5 Output Impedance
The VRM64 series incorporates a resistive output load line so that the output voltage will drop slightly (droop) with increasing output current. This is a desirable characteristic because it allows additional "headroom" for dynamic voltage variations, and is in compliance with the AMD specification. At light loads the output voltage will be at its highest, and the negative voltage transient caused by a sudden increase in output current will be contained within the voltage regulation window. Conversely, at high steady state loads the output voltage will be lower allowing for a positive voltage transient due to a sudden load collapse to be contained within the regulation window.

4.6 Output Overvoltage Protection (OVP)
Circuitry internal to the VRM64 continuously monitors the output voltage for a possible overvoltage condition. The nominal setpoint for this detection is 33% above the VRM's programmed output voltage. When an overvoltage occurs, the VRM64 will output a signal (CB_{OUT}). This signal is at a logic "high" in the event of an overvoltage incident. Details of the drive requirements for this interface can be found in the VRM64 datasheet and in section 8.6 of this application note.

The CB_{OUT} signal can be used within the system to shut down or disconnect the voltage source to the VRM64 and/or activate a user supplied crowbar circuit on the input or output of the converter to clamp the voltage to ground.

Should the output voltage exceed 2.2 V, CB_{OUT} will be forced active high, but not latched. In addition, CB_{OUT} will be forced active high if the output voltage exceeds the VID setting by 33%. This will be a latched condition, requiring a reset by recycling the +12 V. Both protection systems will be operational at the same time as a default. Either or both may be disabled as an option. The overvoltage setting may also be changed for either or both, as an option. Contact the factory for more details.

4.7 Input Over and Undervoltage Protection
The VRMs output will be inhibited when the input voltage is above or below the operating range. Hystersis is provided on both these limits, so that, for example, as the input voltage is increased the output will only be enabled if the input voltage exceeds 10.5 V typ., but then will not be inhibited until the input voltage decreases to below 9.9 V typ.

Whether or not this inhibit is latching will depend on the setting for the current limit latching, see Section 4.12 for more details

4.8 Remote Sense
Two remote sense pins, Vo sen- and Vo sen+ (COREFB L and COREFB H respectively), are provided on the VRM64 converter. These pins are intended to be connected to the point in the system where the output setpoint voltage is to be controlled. Alternatively, the VRM64 may be "locally sensed" by connecting these pins directly to the converter's dc output terminals. The VRM64 is capable of compensating for up to 300 mV drop between the converter's output terminals and the sense point nodes.

The routing and decoupling of the remote sense circuit traces can be critical. See section 8.2 for additional information for connecting the VRM64 both with and without utilization of remote sensing.

4.9 Output Ripple and Noise

This will be critically dependent on the capacitance, ESR and ESL of the output capacitors. See Section 8.5 for the recommended values.

4.10 Output Enable - ENABLE

The output enable (ENABLE) input to the VRM64 converter allows external circuitry to put the VRM64 into a low power dissipation sleep mode. The converter is turned on if the ENABLE pin is high See Figure 2. Pulling the pin low will turn off the unit. There is no pull-up resistor internal to the VRM64 on this pin. Details of the drive requirements for this interface can be found in the VRM64 datasheet and in section 8.6 of this application note.

4.11 Power Good Output - PWRGD

The power good (PWRGD) output is a system flag signaling whether or not the VRM64 output voltage is present and within operational limits as per the AMD specification. The PWRGD signal will go to a low state if the VRM64 output voltage decreases to approximately 140mV below the programmed VID value in accordance with the AMD specification See Figure 3. This is an open-collector output, requiring external pull-up. In accordance with the AMD specification, the PWRGD signal goes high at >2 ms after VDD stabilizes within limits. Details of the drive requirements for this interface can be found in the VRM64 datasheet and in section 8.6 of this application note.

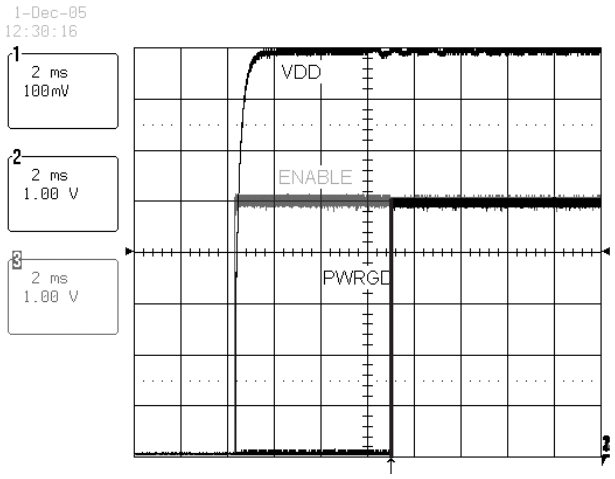

Figure 2 - Power Good On ENABLE

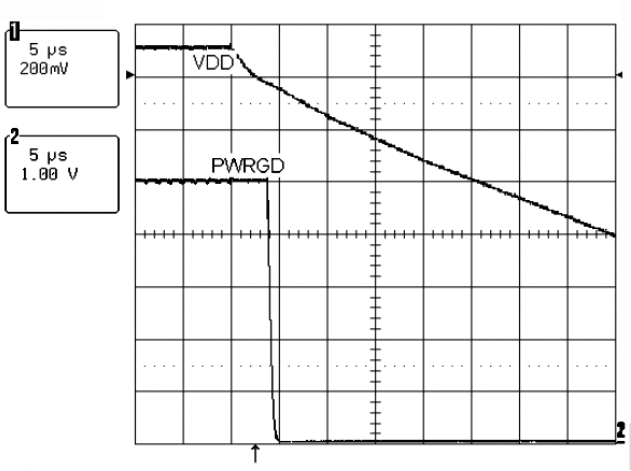

Figure 3 - Power Good Margin at Turn-off, PWRGD stays high until VDD decreases by approximately 140 mV from the set value. (1.5 V, 80 A load)

4.12 Current Limit and Short-Circuit Protection

The VRM64 converter has built-in continuous cycle-by-cycle current limiting and short circuit protection. When the overcurrent limit is reached, the output voltage will drop to near zero. The default setting is at 93 A (typ) and the output will latch off after 10 ms, requiring a reset by recycling the +12 V. However, if this option is chosen, other conditions will also result in a latched-off output. These conditions are: OVLO, UVLO, and an override shutdown command through the SMBus Interface.

The alternative option is a cycle-by-cycle "hiccup" mode, automatic recovery system, operating at 93 A (typ), and limiting the average current to less than 35 A. Contact the factory for this option. When the overload or output short condition is removed, the converter will resume it's voltage regulation function without any user intervention (automatic recovery). There will be some variation in the current limit inception point as a function of operating temperature, component tolerances, etc. The minimum current limit inception point is guaranteed to be above the converter's maximum sustained output current rating over all operating conditions.

4.13 VRM Present Pin

The VRM64 converters provide a pin which signals the system that the converter is plugged into the motherboard.

5. Safety

The VRM64 converter is intended for inclusion in other enclosed equipment and the installer must ensure that it is in compliance with all the safety requirements of the end application. The VRM64 is a high current device. Use appropriate care in handling and installation. There is no isolation between the input and output of the VRM64 converter. The input has internal fuse protection.

The flammability ratings of the converter meet UL94V-0.

6. EMC

The VRM64 converters have been designed for application in end-user equipment that must comply with FCC Class B for conducted emissions and EN55022 Class B for radiated emissions.

7. Use in a Manufacturing Environment

7.1 ESD Control

VRM64 units are manufactured in an ESD controlled environment and supplied in conductive packaging to prevent ESD damage occurring before or during shipping. It is essential that they are unpacked and handled using approved ESD control procedures. Failure to do so could affect the lifetime of the converter.

8. Applications

8.1 Thermal Performance

The electrical operating conditions of the VRM, namely:

- Input voltage, V_{in}
- Output voltage, V_o
- Output current, I_o

determine how much power is dissipated within the converter. Refer to section 8.7 for more information on how these factors influence the conversion efficiency and resultant power dissipation internal to the converter.

After the converter's power dissipation is determined, the resultant thermal stresses should be considered. The stresses most usually considered are operating temperatures of critical internal converter components such as semiconductor junctions and magnetic core temperatures. The following parameters influence the thermal stresses experienced by the converter:

- Ambient temperature at the converter
- Air velocity at the converter
- Actual airflow characteristics at the converter location (i.e. – direction and laminar vs. turbulent)

Note that other parts in the system may block, divert or 'shadow' the airflow to the converter and adversely effect its thermal performance.

In order to simplify the thermal design, derating curves for each of the VRM64 converters are provided in Figure 4. This curve shows the maximum output current as a function of ambient air temperature for a number of different airflow conditions. Note that ambient temperature is the temperature of the air as it arrives at the converter itself and is typically higher than the temperature of the air as it enters the end-user equipment enclosure. The derating curves were generated at the worst case input voltage so that they may be safely used for any input voltage within the specified range. The curves cover airflow conditions in linear feet per minute (LFM) from 300 to 600 (1.5 to 3 m/s). Laminar flow is assumed, as is maximum converter output impedance for the programmable load line model. The derating curve data was taken with the converter oriented so that the airflow enters the converter at pins 1/54 near the fuses and the master controller and exhausts at pins 27/28.

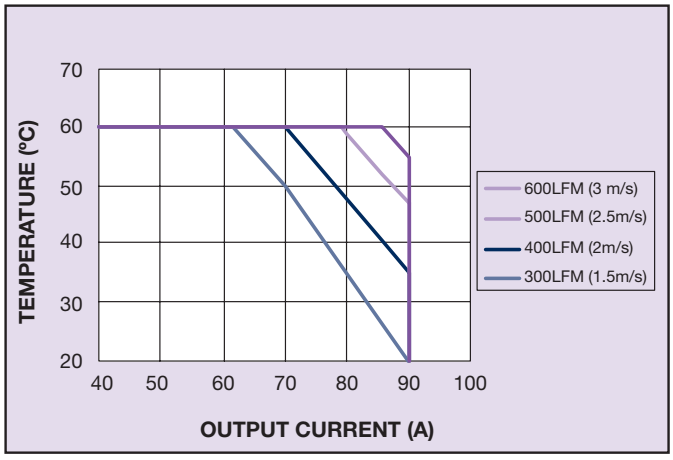

Figure 4 - Typical Thermal Derating At Sea Level (12 Vin, 1.5 Vout)

The figures referenced in the derating curve are intended to provide "ballpark" thermal designs, and will ensure maximum operating hotspot temperatures of 110 ºC internal to the converter under the specified conditions and assumptions. Since every application will be different as far as the airflow characteristics are concerned, a reference 'hot spot' is identified in Figure 5. The temperature at this point must be less than 100 ºC under the worst condition. It is the user's responsibility to measure the converter temperature under actual operating conditions in the system to verify compliance to this maximum temperature. The degree of airflow turbulence, "shadowing" by other components, and the amount of preheating of the ambient air are all factors that are difficult to determine without analysis and measurement in the actual system environment. It is suggested that an IR camera and/or thermocouples be used for this purpose.

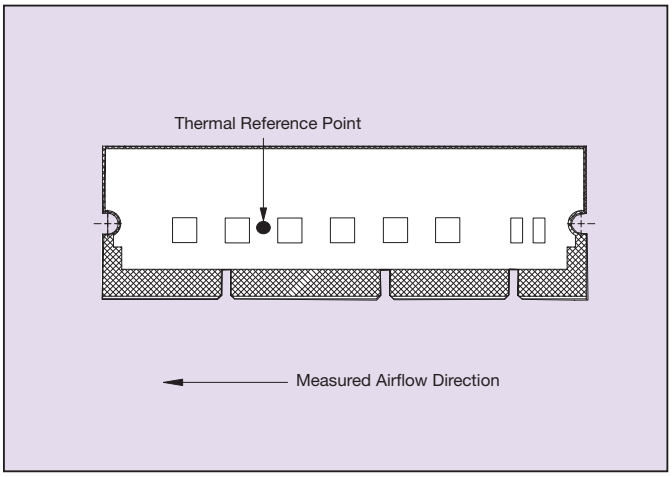

Figure 5 - Hotspot Temperature Check Point

8.2 Remote Sense Compensation

The remote sense compensation feature minimizes the effect of resistance in the distribution system and facilitates accurate voltage regulation at the load terminals or another selected point. The remote sense lines will carry very little current and hence do not require a large cross-sectional area. However, if the sense lines are routed on a PCB, they should be located close to a ground plane and each other in order to minimize any noise coupled onto the lines that might impair control loop stability. The sense line PCB traces should be configured as closely spaced "striplines" with minimum loop area whenever possible. A small 100 nF ceramic capacitor can be connected at the sense point to decouple any noise on the sense wires. The VRM64 converter will compensate for a maximum drop of 300 mV. Remember that when using remote sense compensation all the resistance, parasitic inductance and capacitance of the distribution system are incorporated into the feedback loop of the power module. This can have an effect on the module's compensation capabilities, affecting its stability and dynamic response. Figures 6 and 7 show the recommended converter connections both with and without remote sensing.

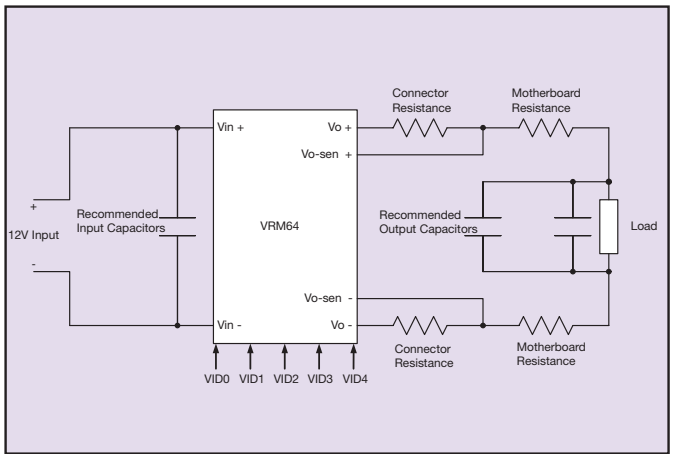

Figure 6 - Recommended Set-up when not using Remote Sense

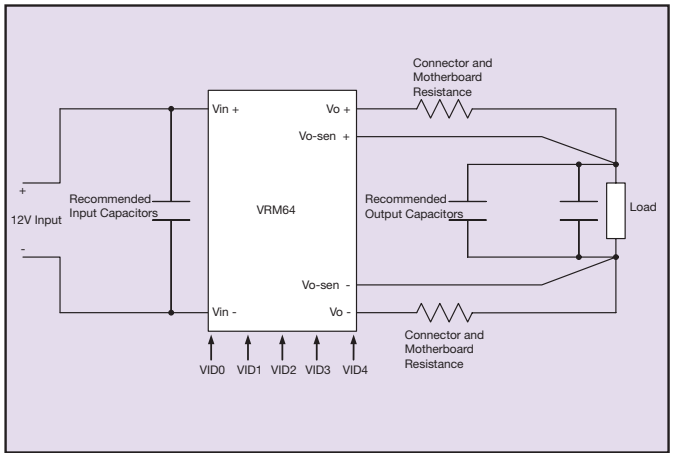

Figure 7 - Recommended Set-up when using Remote Sense

8.3 Input Capacitance

The VRM64 contains some capacitance on its input to minimize ripple current on the input voltage source. However, it is important to use additional decoupling capacitors at the input of the converter to help compensate for the impedance of the input voltage distribution system and provide for stable operation. Artesyn recommends using a minimum of 2 paralleled capacitors of 390 µF each. A capacitor with low ESR and ESL and capable of good ripple current performance should be selected. The maximum reflected current ripple is 4 Arms.

8.4 Output Capacitance

The VRM64 series is designed to power AMD's latest processors, which have extremely high current slew rates. Most of this current slew rate is handled by low ESR capacitors placed as close to the processor as possible. Consequently, the current slew rate will be maximum right at the processor chip die and less at the microprocessor connector. The slew rates referred to in this application note and in the VRM64 datasheet are measured at the output capacitor. The VRM64's output voltage is specified to stay within the regulation limits up to 100 A/us slew rates with the recommended output capacitor configurations. The recommended output capacitance configuration consists of 48 x 22 µF ceramic MLCC such as AVX12106Z226KAT2A

The ESR and ESL of the output capacitors are more important than the amount of capacitance.

Alternative capacitor types and dielectric materials may be substituted, but the resultant total minimum capacitance value, and maximum ESR and ESL must be maintained in order to guarantee proper performance of the processor and the converter's dynamic response. For example, combinations of aluminum polimer, electrolytic, poscap, tantalum, or niobium units may be used with MLCC capacitor population.

The placement and interconnection of the capacitors is critical. As much capacitance as possible should be located in proximity to the microprocessor chip, including the area within the microprocessor socket. As many MLCCs as possible be placed inside the chip socket area.

Without attention to the layout detail, it is possible to inject as much ESR and ESL in the interconnects from the capacitor to the power plane as exists in the component itself. It is important to use very wide and short PCB traces when interconnecting the capacitors. Ideally, no trace at all should be used. Instead, use multiple vias directly from the capacitor mounting pad to the PCB power multiple, plane and ground plane. The maximum system capacitance should not exceed 5,000 µF if VID-on-the-fly operation is required. (See Section 8.6)

8.5 Output Voltage Adjustment

The output voltage of the VRM64 can be set between 0.8 V and 1.55 V by means of a 5 bit Voltage Identification Input (VID) code in 25 mV steps. Note that the setpoint voltage is the upper limit of the output voltage regulation window and that the actual measured output voltage will typically be lower than the setpoint voltage depending upon the converter output resistance, the load current, and regulation effects.

Details of the drive requirements for this interface can be found in the VRM64 datasheet and in section 8.6 of this application note.

The VID codes are shown in Table 2.

8.6 VID-On-The-Fly

The speed of the output respnse to a VID-on-the-fly command will be at approximately 3,000 V/sec. It is set to this figure to ensure that the output response will keep up with the VID-on-the-fly command even with extra load capacitance and high output currents. This is a consequence of

$$\frac{\partial V}{\partial T} = \frac{\partial I}{C}$$

Where ∂I, the current available to change the output voltage is limited by the current limit circuit.

The power good signal will remain high during VID-on-the-fly operation at 80 A load as long as the deviation is <500 mV, even with a load capacitance as high as 5,000 µF see Figures 8 and 9.

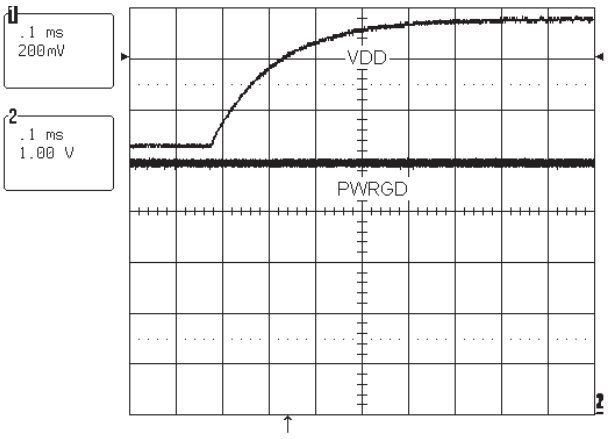

Figure 8 - shows PWRGD staying high whilst VDD changes by 500 mV from 1.05 V to 1.55 V at 80 A load, following an instantaneous VID-on-the-fly command of 00000 from 10100.

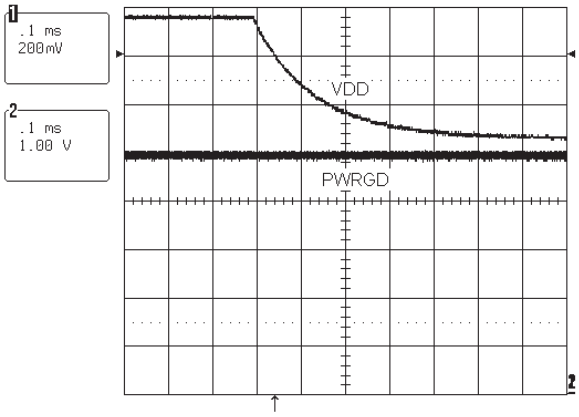

Figure 9 - shows PWRGD staying high whilst VDD changes by 500 mV from 1.55 V to 1.05 V at 80 A load, following an instantaneous VID-on-the-fly command of 10100 from 00000.

VOLTAGE IDENTIFICATION (VID) CODES					
VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	0.800
1	1	1	0	1	0.825
1	1	1	0	0	0.850
1	1	0	1	1	0.875
1	1	0	1	0	0.900
1	1	0	0	1	0.925
1	1	0	0	0	0.950
1	0	1	1	1	0.975
1	0	1	1	0	1.000
1	0	1	0	1	1.025
1	0	1	0	0	1.050
1	0	0	1	1	1.075
1	0	0	1	0	1.100
1	0	0	0	1	1.125
1	0	0	0	0	1.150
0	1	1	1	1	1.175
0	1	1	1	0	1.200
0	1	1	0	1	1.225
0	1	1	0	0	1.250
0	1	0	1	1	1.275
0	1	0	1	0	1.300
0	1	0	0	1	1.325
0	1	0	0	0	1.350
0	0	1	1	1	1.375
0	0	1	1	0	1.400
0	0	1	0	1	1.425
0	0	1	0	0	1.450
0	0	0	1	1	1.475
0	0	0	1	0	1.500
0	0	0	0	1	1.525
0	0	0	0	0	1.550

Table 2 - VID Code Tables

8.7 Control and Status Pin Interfaces

There are several control and status interfaces to the VRM64 converter as described in the datasheet and summarized in Table 4 below.

PIN	Input/ Output	Low Level	High Level
VID (5 bits)	Input	Bit OFF	Bit ON
ENABLE	Input	Converter OFF	Converter ON
PWRGD	Output	Power good FAULT	OK
CB_{OUT}	Output	OK	overvoltage FAULT
-VRMpres	Output	VRM Installed	No VRM

Table 3 - VRM64 Control and Status Interfaces

Unless otherwise noted below, the logic low levels for the interfaces are defined as -0.3 V to 0.4 V and the logic high levels are defined as 0.8 V to 5.5 V.

8.7.1 VID – The VID inputs can be driven with a logic gate for dynamic converter voltage programming. The low and high level voltage ranges are as described above. The power good signal will remain high during VID-on-the-fly operation as long as the deviation is <400 mV.

8.7.2 ENABLE – The ENABLE input can be driven with a logic gate or by a discrete transistor with an external pullup resistor to 5.5 V or less. The VRM64 presents a high input resistance on the ENABLE pin, and contains no internal pullup resistor. It is important to not let this pin float – it must be actively driven to either a low or high level. The low and high level voltage ranges are as described above.

8.7.3 PWRGD – The PWRGD output is an open collector. The PWRGD pin should be externally tied to a maximum voltage of 5.5 V with a pullup resistor or used to drive a logic gate with an input current source. The internal driver can sink a maximum of 5 mA at 0.4 V, and the pullup resistor should be sized accordingly.

PIN NO.	LOGIC I/O	SUMMARY (As Per AMD® OPTERON™ SPECIFICATIONS
8	PWRGD	Open drain, needs external pull-up. Active low if output voltage >140 mV less than the VID set voltage
9	ENABLE	TTL high for enable, low for output inhibited. Needs external pull-up
7	COREFB_H	Remote sensing on output positive
48	COREFB_L	Remote sensing on output negative
49	I_{SHARE}	Current share connection between VRMs (not part of the AMD specification)
47	$CB_{\_OUT}$	Active high for overvoltage and overtemperature
12	SGND	Signal Ground
44	VRMPRES	<1R0 to ground for VRM present
6	VID0	Core voltage setting bit, LSB
50	VID1	Core voltage setting bit
5	VID2	Core voltage setting bit
51	VID3	Core voltage setting bit
4	VID4	Core voltage setting bit, MSB
46	ADD_0	SMBus Address select, internal 1 K resistor to ground fitted
45	ADD_1	SMBus Address select, internal 1 K resistor to ground fitted
11	SM_{CL}	SMBus Clock, internal 5k6 resistor to +5_ALWAYS fitted
10	SM_{DA}	SMBus Clock, internal 5k6 resistor to +5_ALWAYS fitted

Table 4 - Logic I/0

8.7.4 CB_{OUT} (OVP) – The OVP output goes high (5.5 V nominal) in the event of an overvoltage fault. This output provides a low impedance active drive so that devices such as SCR gates may be directly driven if desired. The current being pulled from the VRM CB_{OUT} pins should not exceed 20 mA.

8.7.5 -VRMpres – The VRM64 -VRMpres output is a direct connection to the common ground return internal to the VRM, and can sink at least 100 mA. This closure can easily be sensed by an external logic gate or discrete circuit with an input pullup or current source.

8.8 Efficiency

Because of the high current levels demanded of the VRM64 converters and their placement on the user's motherboard, it is important that they operate as efficiently as possible. A fraction of a percent lower efficiency can result in significant additional power dissipation as well as increased stresses on the converter components. Consequently, the VRM64 was designed to achieve high levels of conversion efficiency. This was accomplished by a combination of topology selection, high levels of integration, component choices and advanced packaging and thermal designs.

A detailed plot of typical efficiency for the VRM64 converters are presented in Figure 10.

Note that there are other sources of power dissipation in addition to the converter's internal dissipation. For example, resistive losses in the user's motherboard PCB traces and connector system at high output currents can be appreciable and must be added to the converter losses when calculating the total system input power and current.

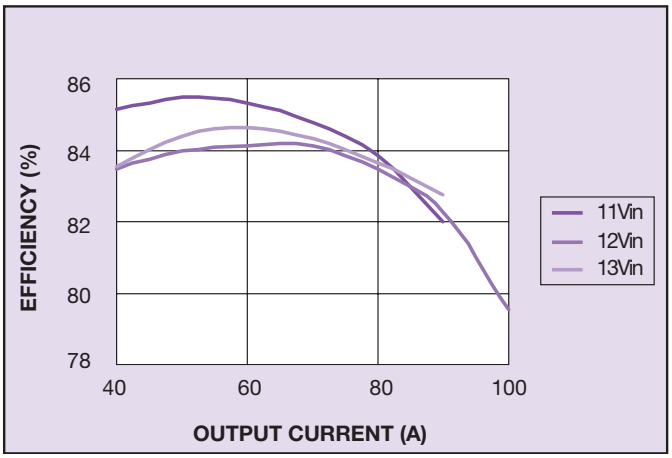

Figure 10 - Efficiency vs. Iout, Vin, VID = 1.5 V

8.9 Transient Response Performance

Excellent converter dynamic response is critical to meet the transient requirements of the Intel VRM64 specification. The advanced design of the Artesyn VRM64 converter, in conjunction with the recommended output capacitor configuration discussed in section 8.5, allows operation at very high current slew rates.

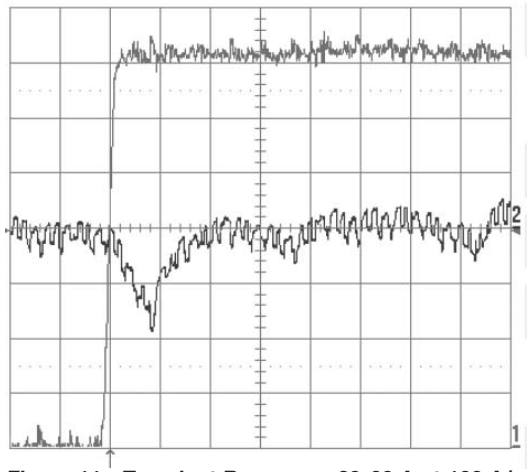

Figure 11 - Transient Response, 20-60 A at 100 A/µ Output Voltage 20 mV/Square, 2 µs/Square

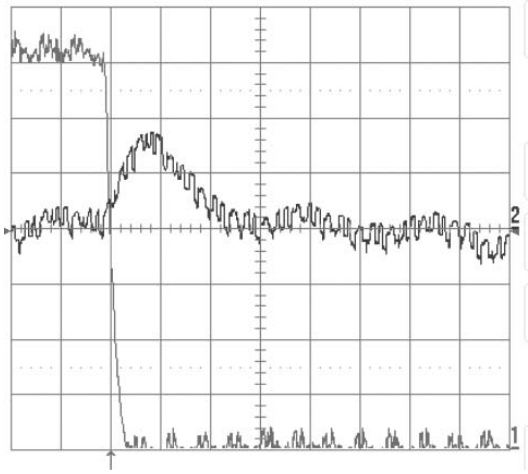

Figure 12 - Transient Response 60 A to 20 A at 100 A/µ Output Voltage 20 mV/Square, 2 µs/Square

9. SMBus INTERFACE

The VRM64 includes a serial bus interface (SMBus) that supports advanced regulator monitoring and control capabilities.

The following regulator monitoring information is available over the SMBus interface:

- Average regulator output current
- Maximum regulator output current, based on system configuration
- Master controller junction temperature
- Number of active regulator phases
- Status of power good signal
- Status of input undervoltage monitor
- Status of input overvoltage monitor
- Status of output overvoltage monitor
- Status of output enable signal
- VID code settings
- Controller ID number
- Controller revision number

The following regulator control capabilities are supported over the SMBus interface:

- Override the VID code settings to program the output voltage
- Override the OE (ENABLE) signal to shutdown the regulator

Note: Both SMBus override commands require writing to a specia‌L ‘lock code’ register first to prevent accidental or noise-induced override commands from being issued to the regulator.

As per the SMBus specification version 2.0 a Slave-receiver is a device that acts as a bus slave in an SMBus transaction while it is receiving address, command or other data from a device acting as a Bus Master in the transaction. A Slave-transmitter is a device acting as a bus slave in an SMBus transaction while it is transmitting data on the bus in a response to a Bus Master’s request.

The VRM64 can act as a Slave-receiver or a Slave-transmitter, but note that it cannot initiate SMBus transactions or drive the clock.

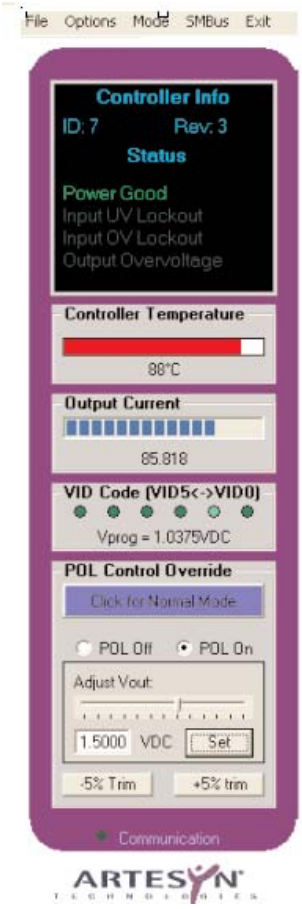

Figure 13 - Typical Computer Display Using the Artesyn Smart SMBus Controller (not part of the AMD VRM) Showing Some of the Features.

Note that this display will be hardware and software dependent

The following sections assume basic familiarity with the SMBus interface. Additional background information is available at http://www.smbus.org.

9.0 SMBus Continued.
The SMBus interface supports the following subset of the SMBus 2.0 specification (appropriate section numbers in parentheses):

- Compliant with 3.3 V to 5 V +/-10% supply levels (2.0)
- SMBus slave support only
- No packet error checking (PEC) (5.4)
- No support for Address Resolution Protocol (5.6)
- Two BUS_ADD[1:0] pins allow unique addressing of four modules per bus
- Supports SMBus protocols:
  – Write byte/word (5.5.4)
  – Read byte/word (5.5.5)

The SMBus slave address is determined by the configuration of the controller BUS_ADD[1:0] pins The read/write (R/W) bit should be set equal to '1' when reading and '0' when writing:

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	0	BUS_ADD1	BUS_ADD0	R/W

Table 5 - Slave Address Byte

9.1 Status Information
Regulator status information is read from register address 00011000. This information is interpreted as follows:

- The PHASE[0:2] bits report the number of active regulator phases (0-5).
- The PG bit reports the status of the Power Good signal.
- The I_UVLO bit reports the status of the input undervoltage comparator.
- The I_OVLO bit reports the status of the input overvoltage comparator.
- The O_OVLO bit reports the status of the output overvoltage comparator.
- The OE bit reports the status of the output enable signal.

B7	B6	B5	B4	B3	B2	B1	B0
PHASE2	PHASE1	PHASE0	PG	I_UVLO	I_OVLO	O_OVLO	OE

Table 6 - Status Byte (Command Code 00011000)

9.2 Average Regulator Output Current
The average regulator output current value is read from register addresses 00010001 through 00010011 (3 bytes). The result is an unsigned number representing the average output current during a 16ms interval. The "data read" bit indicates whether this value has been read since it was last updated. A '1' indicates the value has been read since the last update; a '0' indicates it has not been read. The actual current in Amps is the number read times 112.

B7	B6	B5	B4	B3	B2	B1	B0
BYTE 1 (COMMAND CODE 00010000)							
0	0	0	0	Data Read	IAVG18	IAVG17	IAVG16
BYTE 2 (COMMAND CODE 00010010)							
IAVG15	IAVG14	IAVG13	IAVG12	IAVG11	IAVG10	IAVG9	IAVG8
BYTE 3 (COMMAND CODE 00010011)							
IAVG7	IAVG6	IAVG5	IAVG4	IAVG3	IAVG2	IAVG1	IAVG0

Table 7 - Average Output Current

9.3 Maximum Regulator Output Current
The maximum regulator output current value is read from register addresses 00010100 through 00010110 (3 bytes). The result is an unsigned number representing the maximum regulator output current based on the system configuration. The actual current in Amps is the number read times 112.

B7	B6	B5	B4	B3	B2	B1	B0
BYTE 1 (COMMAND CODE 00010000)							
0	0	0	0	0	IMAX18	IMAX17	IMAX16
BYTE 2 (COMMAND CODE 00010010)							
IMAX15	IMAX14	IMAX13	IMAX12	IMAX11	IMAX10	IMAX9	IMAX8
BYTE 3 (COMMAND CODE 00010011)							
IMAX7	IMAX6	IMAX5	IMAX4	IMAX3	IMAX2	IMAX1	IMAX0

Table 8 - Maximum Output Current

9.4 Master Controller Junction Temperature
The master controller junction temperature value is read from register address 00010111. The result is a two's complement representation of the die temperature (in degrees Celsius).

B7	B6	B5	B4	B3	B2	B1	B0
TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0

Table 9 - Temperature Byte (Command Code 00010111)

9.5 VID Code Settings
VID code settings are read from register address 00011100.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	VID5	VID4	VID3	VID2	VID1	VID0

Table 10 - VID Code Bye (Command Code 00011100)

9.6 Controller ID
The controller ID is read from register address 00011010.This is an 8-bit ID number.

B7	B6	B5	B4	B3	B2	B1	B0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Table 11 - Controller ID Byte (Command Code 00011010)

9.7 Controller Revision
The controller revision is read from register address 00011011. This is an 8-bit REV number.

B7	B6	B5	B4	B3	B2	B1	B0
REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

Table 12 - Controller Revision Byte (Command Code 00011011)

9.8 Regulator Override Commands

The SMBus interface can be used to override regulator operation. In order to override normal operation and shutdown the regulator or program the output voltage, two steps must be taken: First, the Lock Code byte must be written at register address 00011101 with the value LC[7:0] = '01010101'.

B7	B6	B5	B4	B3	B2	B1	B0
LC7	LC6	LC5	LC4	LC3	LC2	LC1	LC0

Table 13 - Lock Code Byte (Command Code 00011101)

Next, the Override Command byte must be written at register address 00011001 with the appropriate value. If the shutdown bit is set to '1', the regulator is shutdown. If the VID override (VO) bit is set to '1' then the nominal output voltage (VNOM pin) is set to VNOM = 450 mV + 25 mV*DAC[5:0].

B7	B6	B5	B4	B3	B2	B1	B0
SD	VO	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

Table 14 - Override Command Byte (Command Code 00011001)

REGISTER ADDRESS (COMMAND CODE)	NAME	READ/WRITE	UNIT	DESCRIPTION
00010001 to 00010011	Average Output Current	Read	1 mA	Average system output current. Includes a "data read" bit indicating whether this values
00010100 to 00010110	Maximum Output Current	Read	1 mA	Maximum system output current based on current configuration
00010111	Controller Junction Temperature	Read	1 °C	Master controller junction temperature
00011000	Status	Read	N/A	Regulator status information
00011100	VID Settings	Read	N/A	VID codes settings
00011010	Controller ID	Read	N/A	Controller ID number
00011011	Controller Revision	Read	N/A	Controller revision number
00011101	Lock Code	Read/Write	N/A	"01010101" must be written to this register before other registers can be written to
00011001	Override Command	Read/Write	N/A	Disables regulator or programs output voltage. Must write to Lock Code register before writing to this register

Table 15 - Summary