COMPUTING

MVME8100/MVME8105/MVME8110

Programmer's Reference

P/N: 6806800P28H

April 2019

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EMBEDDED TECHNOLOGIES

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Overview of Contents

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Chapter 1, Introduction on page 13 provides a brief product description and block diagrams showing the architecture of the MVME8100/MVME8105/MVME8110.

Chapter 2, Memory Maps on page 21, provides information on the memory map.

Chapter 3, Register Descriptions on page 23, contains status registers for the system resources.

Chapter 4, Programming Model on page 35, includes additional programming model for the board.

Chapter 5, Boot System on page 39, provides information on the U-boot.

Appendix A, Related Documentation on page 47, provides a listing of related Artesyn Embedded Technologies manuals, vendor documentation, and industry specifications.

Abbreviations

This document uses the following abbreviations:

Acronym	Description
BCD	Binary Coded Decimal
CPLD	Complex Programmable Logic Device
CRC	Cyclic Redundancy Check
eLBC	Enhanced local bus controller
EEPROM	Electrically Erasable Programmable Read Only Memory
Flash	Flash Memory
LBC	Local Bus Controller
MMC	Module Management Controller
MRAM	Magneto resistive Random Access Memory

Acronym	Description (continued)
PCIe	Peripheral Component Interconnect Express
PIC	Programmable Interrupt Controller
RTC	Real Time Clock
SATA	Serial ATA
SBC	Single Board Computer
SSCR	Sticky Scratch Register
SPD	Serial Presence Detect
SRIO	Serial Rapid IO
VME	VMEbus (Versa Module Eurocard)
VPD	Vital Product Data

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu

Notation	Description (continued)
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury.
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	Indicates a property damage message.
	Helpful information and tips.

Summary of Changes

Part Number	Publication Date	Description
6806800P28H	April 2019	Updated to new Artesyn format; minor grammar and formatting updates throughout document; converted bulleted lists of features into a comparison table; Freescale changed to NXP. Removed Board Variants and Board Accessories tables; added product data sheets to list of related documentation in Appendix A.
6806800P28G	October 2015	Added MVME8105 to MVME81xx family. Updated the document with MVME8105 information.
6806800P28F	September 2015	Updated Tables *CPLD Command/Status Register*, *User LED Control Register,* and *Tick Timer Control Register.*
6806800P28E	September, 2014	Changed title as MVME8100 / MVME8110. Added information about MVME8110.
6806800P28D	June, 2014	Re-branded to Artesyn template.
6806800P28C	October, 2013	Updated *Boot Options on page 40*.
6806800P28B	September, 2012	Updated *Enhanced Local Bus Register on page 24*, *Identification Register on page 25*, *CPLD Command/Status Register on page 26*, *User LED Control Register on page 30*, and *RTM GPIO Register on page 34*. Added *CPLD Build Code Register on page 31*.
6806800P28A	May, 2012	First Release

1.1 Overview

This chapter describes the board level hardware features of the MVME8100, MVME8105 and MVME8110 single board computers. Refer to *P5020 Reference Manual* listed in *Appendix A on page 47*, for more detail and programming information.

The MVME8100 single board computer is a VMEbus board based on the NXP® QorIQ® P5020 processor. It is a high performance 6U VME/VXS board targeted towards high-end military and industrial automation applications using VMEbus technology. The MVME8100 is compliant with the VMEbus International Trade Association (VITA) standards VMEbus, 2eSST, and PCI-X. The MVME8100 can accommodate two PCI/PCI Express Mezzanine Cards (PMC/XMC).

The MVME8105 is a dual core non-VXS version of the MVME8100 board based on the NXP QorIQ P5020 processor. It runs at 2.0GHz with 4GB DDR3. The MVME8105 provides a second 1000Base-TX RJ-45 interface on the front panel.

The MVME8110 is a single core non-VXS version of the MVME8100 board based on the NXP QorIQ P5010 processor. It runs at 1.2GHz with 2GB DDR3.

1.2 Feature Summary

The following table provides a summary of features for all three board variations. Not all processor features are implemented on the board.

Table 1-1 Board Feature Summary

Feature	MVME 8100	MVME 8105	MVME 8110
NXP® QorIQ®Processor	P5020 (1.8/2GHz)	P5020 (2.0GHz)	P5010 (1.2GHz)
e5500 cores	2	2	1
10GBE (XAIU) controllers	1	1	1
1GbE controllers (SGMII and RGMII)	5	5	5
64-bit DDR3/3L SDRAM memory controllers with ECC	2	2	1
Programmable Interrupt Controller (PIC)	Y	Y	Y
I^2C controllers	4	4	4
2-pin/4-pin UARTs	4/2	4/2	4/2
4-channel DMA engines	2	2	2
Enhanced local bus controller	1	1	1
PCI Express 2.0 controller/ports	4	4	4
Serial Rapid IO controller/ports v1.3 compliant with features of v2.1)	2	2	2
Enhanced secure digital host controller (SD/MMC)	1	1	1
Enhanced Serial Peripheral Interfaces (eSPI with four chip selects)	1	1	1
High-speed USB 2.0 controllers with integrated PHYs	2	2	2
CoreNet platform cache with ECC	2Mbyte	2Mbyte	1Mbyte
SATA 2.0 controller	2	2	2
RAID5/6 engine	1	1	1
SEC encryption	Y	N	N
System Memory			
DDR3 SDRAM with ECC	4GB	4GB	2GB
DDR3 data rate	1333MT/s	1333MT/s	1200MT/s
SMBus			

Table 1-1 Board Feature Summary (continued)

Feature	MVME 8100	MVME 8105	MVME 8110
512Kbit user configuration serial EEPROM	Y	Y	Y
256B serial presence detect (SPD) EEPROMs	Y	Y	Y
64Kbit Vital Product Data (VPD) EEPROM	Y	Y	Y
Real Time Clock (RTC) with battery backup**	Y	Y	Y
Temperature sensors	Y	Y	Y
RTM and XMC VPD EEPROMs	Y	Y	Y
Flash			
Soldered SPI Flash, 8MB each, switchable for uboot primary/backup support	2	2	2
Hardware switch or software bit write protection for entire logical bank	Y	Y	Y
eMMC Flash	8GB	8GB	8GB
NVRAM			
Magneto resistive Random Access Memory (MRAM)	512KB	512KB	512KB
PCI Express			
4x ports to VXS backplane P0 (muxed with SRIO ports)	2	-	-
8x port to PMC/XMC Site 1	1	1	1
4x port to PMC/XMC Site 2	1	1	1
SRIO - 4x ports to VXS backplane P0 (muxed with PCIe ports)	2	-	-
USB			
USB 2.0 for front panel I/O	1	-	1
USB 2.0 for backplane RTM I/O	2	2	2
Ethernet			
10/100/1000BASE-T Ethernet port to front panel	1*	2	1
10/100/1000BASE-T Ethernet channels to P2/RTM	2	1	2
1000BASE-BX Ethernet SERDES channels to P0 backplane/RTM	2	-	-
SATA Ports			
SATA Gen 3 ports to P0 backplane/RTM	2	-	-
Serial Ports			

Table 1-1 Board Feature Summary (continued)

Feature	MVME 8100	MVME 8105	MVME 8110
RS-232/422/485 console port to front panel or P2/RTM	1	1	1
RS-232/422/485 COM ports to P2/RTM	Up to 4	Up to 4	Up to 4
VMEbus - VME64x and 2eSST	Y	Y	Y
Timers			
32-bit timers in CPU	8	8	8
Watchdog timer in CPU	Y	Y	Y
PMC/XMC sites with 64-bit PMCIO on Site 1	2	2	2
Option for 2.5" SATA SSD (PMC/XMC Site 2)	Y	Y	Y
GPIO Interface to RTM/P0	4	2	2
VXS Interface			
VITA 41 specification compliant	Y	Y	Y
Supports backplane P0 connector	Y	-	-
Form Factor			
Standard 6U, one slot	Y	Y	Y
Support 0.8 and 0.85 inch slot chassis	Y	Y	Y
Support heat frame on both sides for conduction cooled board	Y	Y	Y
Software Support			
VxWorks	Y	Y	Y
Linux	Y	Y	Y
Compatible with RTM (assembly # 0106852M***)	Y	Y	Y
I/O			
Micro DB-9 connector for console port on front panel	1*	1	1
USB 2.0 Type A connector on front panel	1*	-	1
Front panel RJ-45 connector with integrated LEDs for 10/100/1000 Ethernet channel	1*	2	1
PMC/XMC Site 1 front I/O and rear PMC I/O	Y	Y	Y
PMC/XMC Site 2 front I/O	Y	Y	Y
Serial ports to P2/RTM, (two Micro DB-9 connectors on RTM panel and two on planar headers)	4	4	4

Table 1-1 Board Feature Summary (continued)

Feature	MVME 8100	MVME 8105	MVME 8110
10/100/1000BASE-T Ethernet channels to RJ-45 connectors on RTM panel	2	1	2
1000BASE-BX Ethernet SERDES channels to backplane	2	-	-
USB 2.0 ports to RTM with USB Type A connectors on RTM panel	2	2	2
SATA port to RTM with eSATA connector on RTM	2	-	-
GPIOs to planar headers on RTM (**See note below**)	4	2	2
Other Features			
Front panel RESET switch	Y	Y	Y
LED front panel status indicators (four user/fail/ready LEDs)	Y	Y	Y
Planar status indicators	Y	Y	Y
Boundary scan support	Y	Y	Y

*Not present in ENP4 version

**Battery not present in ENP4 version

NOTE: The front panel I/O connectors are available only in ENP1 (air cooled variants). I/O signals in the ENP4 (conduction cooled) variant are accessed through P2 only

1.3 Ordering and Support Information

The data sheets for the MVME8100, MVME8105 and MVME8110 boards contain a complete list of available variants and accessories. Refer to *Appendix A Related Documentation* or consult your local Artesyn sales representative for the availability of product variants.

For technical assistance contact your local Artesyn sales representative or visit http://crcportal.artesyn.com.

Report any issues of product damage or shortages to our Contact Center at RMAsupport.ec@artesyn.com

1.4 Block Diagram

The block diagrams for MVME8100/MVME8105/MVME8110 SBC are shown in the following figures:

Figure 1-1 Block Diagram of MVME8100

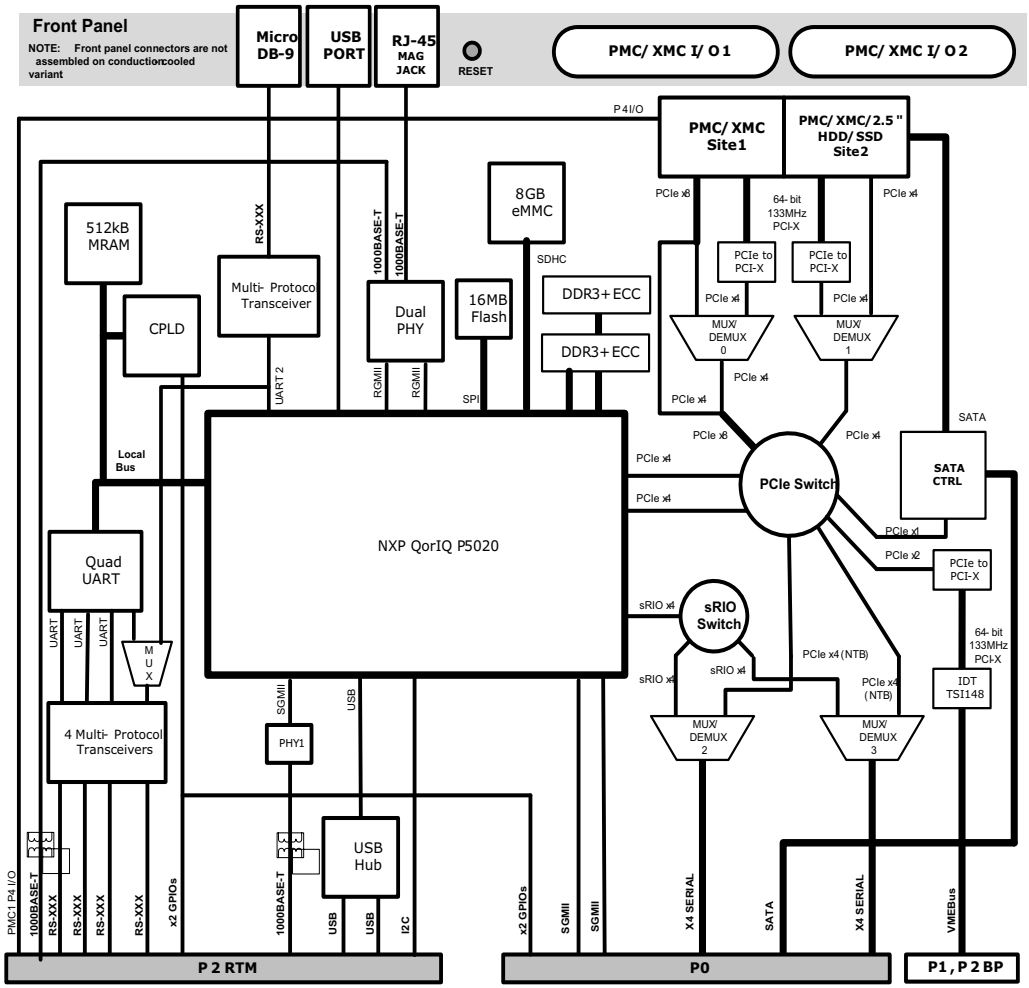


Figure 1-2 Block Diagram of MVME8105

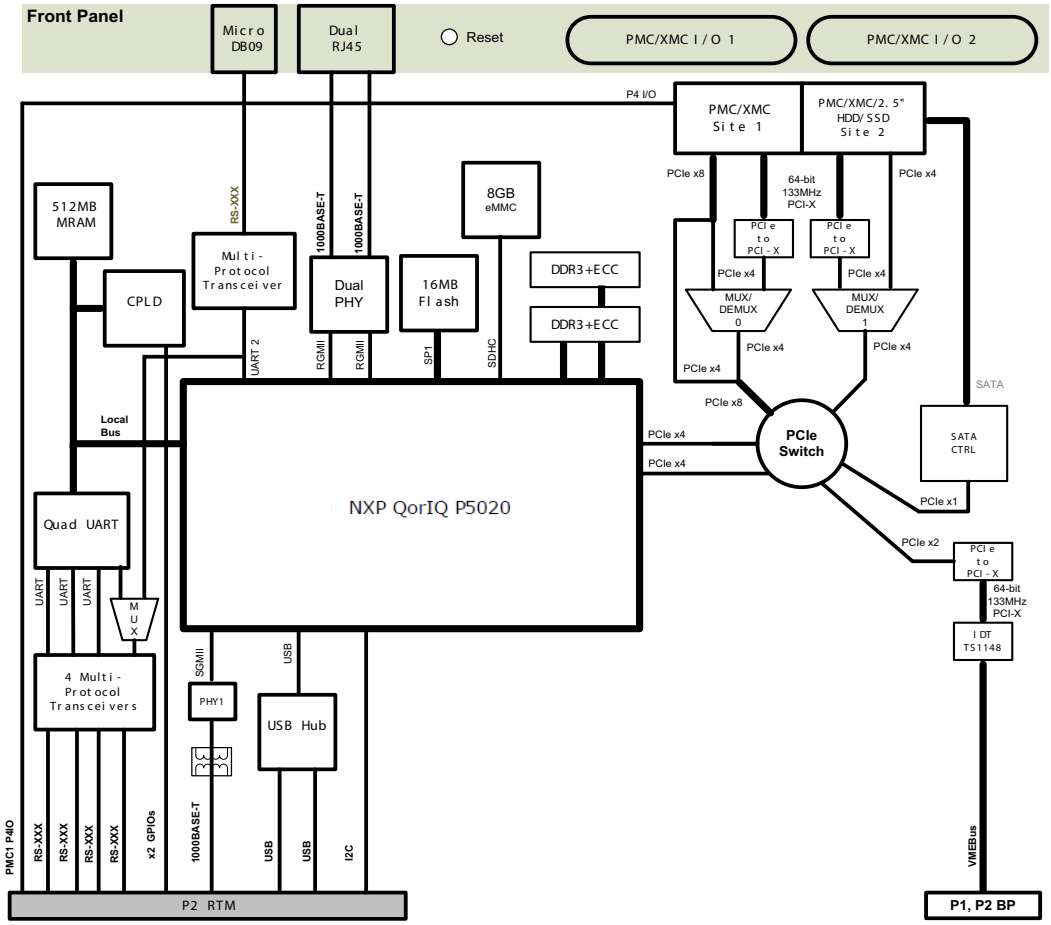
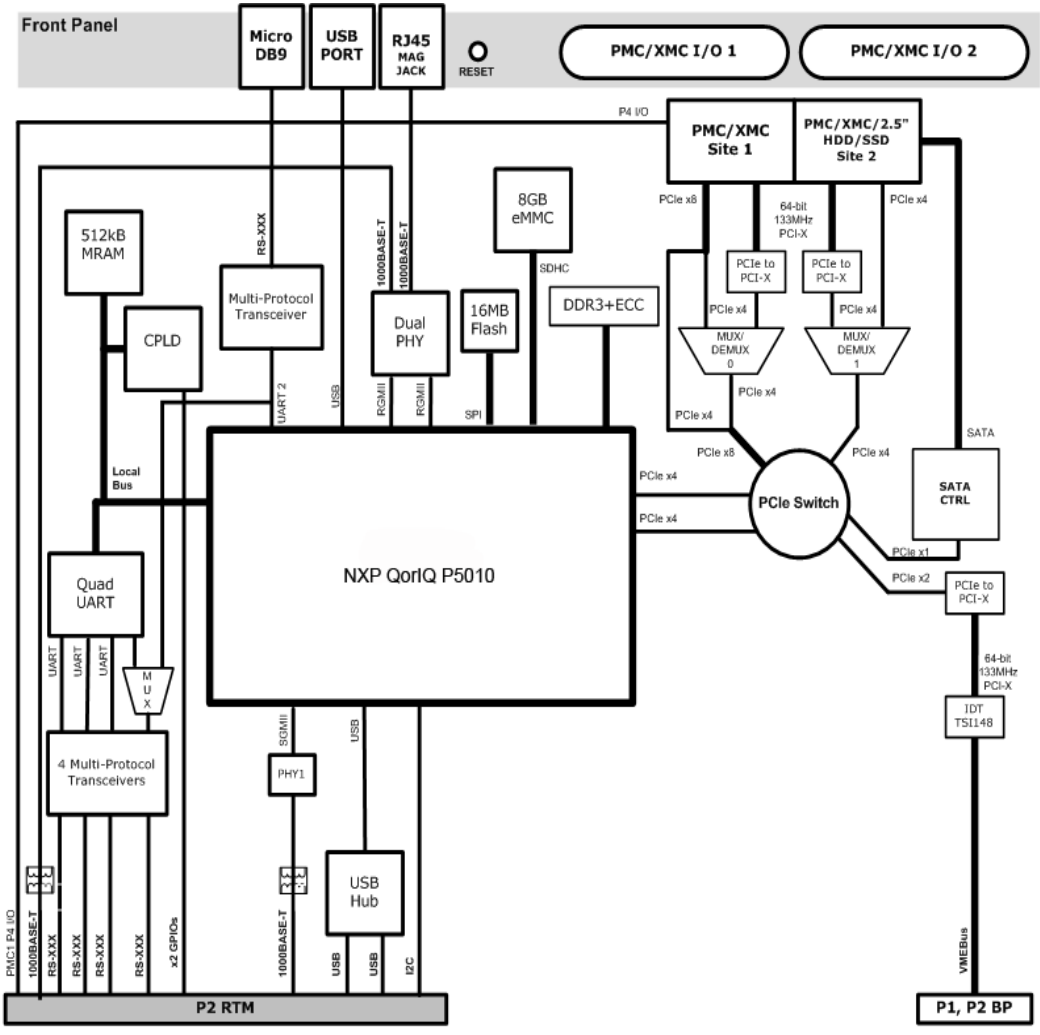


Figure 1-3 Block Diagram of MVME8110



2.1 Overview

This chapter provides the memory mapping addresses for the MVME8100, MVME8105 and MVME8110 boards. Refer to the *P5020/P5010 Reference Manual* for additional details and/or programming information.

2.2 Memory Maps

The following table shows the suggested local memory address map of the P5010/P5020 processors:

Table 2-1 P5010/P5020 Local Memory Mapping (36-bit physical memory map)

Device Name	Start Address	Size
DDR	0x0_0000_0000	8GB
SRIO Mem	0xb_4000_0000	256MB
PCIE 0 Mem	0xc_0000_0000	2GB
PCIE 1 Mem	0xc_8000_0000	2GB
PCIE 0 Mem Prefetch	0xd_8000_0000	2GB
PCIE 1 Mem Prefetch	0xe_0000_0000	2GB
DCSR	0xf_f000_0000	4MB
BMAN	0xf_f400_0000	2MB
QMAN	0xf_f420_0000	2MB
MRAM	0xf_f500_0000	512KB
UART1	0xf_f508_0000	64KB
UART2	0xf_f509_0000	64KB
UART3	0xf_f50a_0000	64KB
UART4	0xf_f50b_0000	64KB
PCI0 IO	0xf_f800_0000	64KB
PCI1 IO	0xf_f900_0000	64KB
CPLD	0xf_ffdf_0000	64KB

NOTES

3.1 Overview

This chapter describes the various registers on the MVME8100/MVME8105/MVME8110 boards.

3.2 CPLD Registers

For the Complex Programmable Logic Device (CPLD) register description, the convention shown in the following tables are used.

Table 3-1 Register Defaults

Default	Description
-	Not applicable or undefined
0 or 1	Default value after configuration
Undef	Undefined value
<reset>: 0 or 1	Default value after deassertion of the reset signal <reset>
Ext	External Switch Source. Default depends on external switch setting.

Table 3-2 Register Access Type

Access	Description
LBC:r	Read only through LBC connection to CPU
LBC:w	Write only through LBC connection to CPU
LBC:r/w	Read and write through LBC connection to CPU
LBC:r/w1c	Read and write-1-to-clear, write 0 has no effect through LBC connection to CPU

3.2.1 Enhanced Local Bus Register

The following table shows how the Enhanced Local Bus registers are memory mapped in the CPU.

Table 3-3 Enhanced Local Bus Register Overview

Offset	Description
0x00	Identification Register
0x04	CPLD Command/Status Register
0x08	User LED Control Registers
0x0C	CPLD Build Code Registers
0x10	Tick Timer1 Control Register
0x14	Tick Timer1 Compare Registers
0x18	Tick Timer1 Counter Registers
0x20	Tick Timer2 Control Register
0x24	Tick Timer2 Compare Registers
0x28	Tick Timer2 Counter Registers
0x30	Tick Timer3 Control Register
0x34	Tick Timer3 Compare Registers
0x38	Tick Timer3 Counter Registers
0x40	Tick Timer4 Control Register
0x44	Tick Timer4 Compare Registers
0x48	Tick Timer4 Counter Registers
0x50	Tick Timer Prescaler Registers
0x60	RTM GPIO Registers
0x80	Scratch Register

3.2.2 Identification Register

Table 3-4 Identification Register

Offset: 0x00			
Bit	**Description**	**Default**	**Access**
0:15	Reserved	8'h00	LBC:r
16:17	Reserved	2'b00	LBC:r
18:19	Unit Variant Code Register state bits directly reflects logic level applied at VARCODE pins VARCODE[1:0]: 00 is MVME8100 ENP1 variant 01 is MVME8100 ENP4 variant 10 is MVME8110 ENP1 variant	Ext	LBC:r
20:21	Board Revision Note: Register state bits directly reflect logic level applied at pins BOARDREV (ex. 2'b01 for rev1.1). This will be used for backward compatibility.	Ext	LBC:r
22:31	Board Identification Register 10'h007: MVME8100 Others: Reserved for future boards	10'b007	LBC:r

3.2.3 CPLD Command/Status Register

Table 3-5 CPLD Command/Status Register

Offset: 0x04 NOTE: Some CPLD Status Registers can be set/cleared using "Write CPLD Command Register".			
Bit	**Description**	**Default**	**Access**
0:31	CPLD Command Register 32'h0000_eea1: Service IWD and enable OSWD 32'h0000_eea2: Clear reset indication flags 32'h0000_eea3: Assert SRIO MCAST 32'h0000_eea5: Enable Abort Interrupt 32'h0000_eea6: Clear Abort Interrupt 32'h0000_eea7: Protect CPU EEPROM Devices 32'h0000_eea8: Enable PCIe Configuration EEPROM address swap 32'h0000_eea9: Enable quad UART invert IRQ 32'h0000_bbc1: Disable Abort Interrupt 32'h0000_bbc2: Disable OSWD 32'h0000_bbc3: Unprotect CPU EEPROM Devices 32'h0000_bbc4: Disable PCIe Configuration EEPROM address swap 32'h0000_bbc5: Disable quad UART invert IRQ 32'h0000_8000: Corrupt LBC Data for 5ms (For test only) Others: Reserved command	-	LBC:w
0	Reserved	1'b0	LBC:r
1	P5020 / P5010 Reset Request indication 1: P5020 / P5010 Reset Request has not generated reset 0: P5020 / P5010 Reset Request has generated reset	1'b1	LBC:r
2	Front panel/Backplane reset switch indication 1: Front panel/Backplane has not generated reset 0: Front panel/Backplane reset has generated reset	1'b1	LBC:r
3	IWD Reset indication 1: IWD Reset has not generated reset 0: IWD Reset has generated reset	1'b1	LBC:r
4	OSWD Reset indication 1: OSWD Reset has not generated reset 0: OSWD Reset has generated reset	1'b1	LBC:r

Table 3-5 CPLD Command/Status Register (continued)

Offset: 0x04 NOTE: Some CPLD Status Registers can be set/cleared using "Write CPLD Command Register".			
Bit	**Description**	**Default**	**Access**
5	VME Reset indication 1: VME Reset has not generated reset 0: VME Reset has generated reset	1'b1	LBC:r
6	Boot from backup flash flag 0: Boot from default/selected flash 1: Boot from backup flash	1'b0	LBC:r
7	P0 Connector Port 2 PCIe/SRIO Fabric Selection 1: Port 2 same as Port 1 selection and is controlled by SW2-8 (SW3-2 open) 0: Port 2 opposite toPort1 selection and is based on S2-8 (SW3-2 closed) Note: The bit reflects SW3-2 setting sampled at reset. (P0 and SRIO is for MVME8100 only)	Ext	LBC:r
8	Watchdog enable/disable. 1: Watchdog controller disabled (SW2-1 open) 0: Watchdog controller enabled (SW2-1 closed) Note: The bit reflects SW2-1 setting sampled at reset.	Ext	LBC:r
9	Clear Environment Variables Pin Status 1: Clear Environment Variables Disabled (SW4-1 open) 0: Clear Environment Variables Enabled (SW4-1 closed) Note: The bit reflects SW4-1 setting sampled at reset.	Ext	LBC:r
10	RTM Detect Register 1: RTM not present 0: RTM present	Ext	LBC:r
11	PCIE/SRIO Root Complex Enable 1: Enabled (Load Root Complex based EEPROM into PCIe and SRIO switches) 0: Disabled (Load Endpoint based EEPROM into PCIe and SRIO switches) Note: The bit reflects SW4-2 setting sampled at reset. (SRIO for MVME8100 only)	Ext	LBC:r

Table 3-5 CPLD Command/Status Register (continued)

Offset: 0x04 NOTE: Some CPLD Status Registers can be set/cleared using "Write CPLD Command Register".			
Bit	**Description**	**Default**	**Access**
12	VME System Controller Enable 1: Automatic Enable/Disable (SW4-3 open). System controller functionality depends on VBG3IN_N signal. 0: Manual Enable/Disable (SW4-3 closed). System controller functionality depends on bit12. Note: The bit reflects SW4-3 setting sampled at reset	Ext	LBC:r
13	VME System Controller Manual Enable 1: System Controller Enabled (SW4-4 open) 0: Non-system Controller Disabled (SW4-4 closed) Note: The bit reflects SW4-4 setting sampled at reset	Ext	LBC:r
14	Quad UART IRQ Inversion 1: Invert quad UART IRQ interrupt levels to CPU (active low IRQ) 0: Normal quad UART IRQ interrupt levels to CPU (active high IRQ)	0'b0	LBC:r
15	P0 Connector PCIE/SRIO Fabric Selection 1: SRIO Fabric (SW2-8 open) 0: PCIe Fabric (SW2-8 closed) Note: The bit reflects SW2-8 setting sampled at reset (P0 and SRIO for MVME8100 only)	Ext	LBC:r
16	XMC1 Detect 1: Not Present 0: Present	Ext	LBC:r
17	XMC2 Detect 1: Not Present 0: Present	Ext	LBC:r
18	PMC1 Detect 1: Not Present 0: Present	Ext	LBC:r
19	PMC2 Detect 1: Not Present 0: Present	Ext	LBC:r

Table 3-5 CPLD Command/Status Register (continued)

Offset: 0x04 NOTE: Some CPLD Status Registers can be set/cleared using "Write CPLD Command Register".			
Bit	**Description**	**Default**	**Access**
20	Abort Interrupt Enable Status 1: Enabled 0: Disabled	1'b0	LBC:r
21	Front panel/Backplane Abort Interrupt flag 1: Front panel/Backplane Abort has NOT asserted interrupt 0: Front panel/Backplane Abort has asserted interrupt	1'b1	LBC:r
22	U-Boot Flash Protection 1: U-boot SPI Flash Unprotected 0: U-boot SPI Flash Protected Note: The bit reflects SW3-1 setting	Ext	LBC:r
23	U-Boot Flash Selection Register 1: Boot from Default Flash (device 0) 0: Boot from Recovery Flash (device 1) Note: The bit reflects SW5-1 setting sampled at reset	Ext	LBC:r
24	Write Protect Status of CPU EEPROMs 0: Unprotected 1: Protected	1'b0	LBC:r
25	PCIe Configuration EEPROM Swap Status 1: PCIe Configuration EEPROM address swap enabled 0: EEPROM address swap disabled	1'b0	LBC:r
26	Serial Console Port Direction 1: Route Serial Console Port to Front Panel Connector (SW2-2 open) 0: Route Serial Console Port to P2 Connector (SW2-2 closed)	Ext	LBC:r
27	Serial Port 0 Mode 1: Serial Port 0 Operates in RS-232 Mode (SW2-3 open) 0: Serial Port 0 Operates in RS-485/422 Mode (SW2-3 closed)	Ext	LBC:r
28	Serial Port 1 Mode 1: Serial Port 1 Operates in RS-232 Mode (SW2-4 open) 0: Serial Port 1 Operates in RS-485/422 Mode (SW2-4 closed)	Ext	LBC:r

Table 3-5 CPLD Command/Status Register (continued)

Offset: 0x04 NOTE: Some CPLD Status Registers can be set/cleared using "Write CPLD Command Register".			
Bit	**Description**	**Default**	**Access**
29	Serial Port 2 Mode 1: Serial Port 2 Operates in RS-232 Mode (SW2-5 open) 0: Serial Port 2 Operates in RS-485/422 Mode (SW2-5 closed)	Ext	LBC:r
30	Serial Port 3 Mode 1: Serial Port 3 Operates in RS-232 Mode (SW2-6 open) 0: Serial Port 3 Operates in RS-485/422 Mode (SW2-6 closed)	Ext	LBC:r
31	Serial Console Port Mode 1: Serial Console Port Operates in RS-232 Mode (SW2-7 open) 0: Serial Console Port Operates in RS-485/422 Mode (SW2-7 closed)	Ext	LBC:r

U-Boot and OS can read bit 8 Clear Environment Pin Status, and use this to clear environment parameters.

3.2.4 User LED Control Register

Table 3-6 User LED Control Register

Offset: 0x08			
Bit	**Description**	**Default**	**Access**
0	User LED 1A (front panel USER 1 bicolor LED, yellow) 1: On 0: Off	0	LBC:r/w
1	User LED 1B (front panel USER 1 bicolor LED, red) 1: On 0: Off	0	LBC:r/w
2	User LED 2 (back side D19 bicolor LED, red) 1: On 0: Off	0	LBC:r/w

Table 3-6 User LED Control Register (continued)

Offset: 0x08			
Bit	**Description**	**Default**	**Access**
3	User LED 3 (back side D19 bicolor LED, yellow) 1: On 0: Off	0	LBC:r/w
4:7	Reserved.	4'h0	LBC:r
8	PS LED 1 (back side D33 LED, red) 1: On 0: Off	0	LBC:r/w
9	PS LED 2 (back side D34 LED, green) 1: On 0: Off	0	LBC:r/w
10	PS LED 3 (back side D35 LED, yellow) 1: On 0: Off	0	LBC:r/w
11	Reserved	0	LBC:r/w
12:31	Reserved	21'h00000	LBC:r

3.2.5 CPLD Build Code Register

This read-only register displays the CPLD build code data.

Table 3-7 CPLD Build Code Register

Offset: 0x0C			
Bit	**Description**	**Default**	**Access**
0:7	Two digit build year (BCD)	8'hxx	LBC:r
8:15	Two digit build month (BCD)	8'hxx	LBC:r
16:23	Two digit build day (BCD)	8'hxx	LBC:r
24:31	Two digit sequence number (BCD)	8'hxx	LBC:r

3.2.6 Tick Timer Register

Table 3-8 Tick Timer Control Register

Offset: 0x10, 0x20, 0x30, 0x40			
Bit	**Description**	**Default**	**Access**
0	Enable counter. When the bit is set, the counter increments. When the bit is cleared, the counter does not increment. Writing a "1" enables the counter	1'b0	LBC:r/w
1	Clear Counter on Compare. When the bit is set, the counter is reset to 0 when it compares with the compare register. When the bit is cleared the counter is not reset.	1'b0	LBC:r/w
2	Clear Overflow Bit. Write 1 to clear overflow counter. Always return 0 when read.	1'b0	LBC:r/w
3	Reserved	1'b0	LBC:r
4:7	Overflow Bits are the output of the overflow counter. It increments each time the tick timer sends an interrupt to the local bus interrupter. The overflow counter can be cleared by writing a 1 to the Clear Overflow bit.	4'h0	LBC:r/w
8	Enable Interrupt. When the bit is set, the interrupt is enabled. When the bit is cleared, the interrupt is not enabled.	1'b0	LBC:r/w
9	Clear Interrupt. Write 1 to clear interrupt. Always return 0 when read.	1'b0	LBC:r/w
10	Interrupt Status. A value of "1" in this bit indicates that a interrupt has been generated by the corresponding timer. A value of "0" indicates that no interrupt has been generated by the corresponding timer.	1'b0	LBC:r
11:31	Reserved	21'h00_0000	LBC:r

Table 3-9 Tick Timer Compare Register

Offset: 0x14, 0x24, 0x34, 0x44			
Bit	**Description**	**Default**	**Access**
0:31	Tick Timer Compare	32'hFFFF_FFFF	LBC:r/w

Table 3-10 Tick Timer Prescaler Register

Offset: 0x50			
Bit	**Description**	**Default**	**Access**
0:7	Prescaler Bits Formula= Prescaler Adjust = 256-(25/CLKOUT(MHz))	8'hE7	LBC:r/w
8:31	Reserved	24'h000_0000	LBC:r

The prescaler register is changed to allow lower resolution for the four 32-bit tick timers. All four 32-bit tick timers use the same prescaler register. By lowering the resolution, the maximum interval for the tick timers to generate an interrupt is increased from 71.6 minutes, at 1MHz to 733.0 minutes, at 97KHz. The default and maximum recommended value for the prescaler register is 0xe7, and the minimum value for the prescaler is zero.

The tick timer counter is compared to the Compare Register. When the values are equal, the tick timer interrupt is asserted and the overflow counter increments. If the clear-on-compare mode is enabled, the counter is also cleared. For periodic interrupts, this equation should be used to calculate the compare value for a specific period (T):

T(us) = (256 - prescaler) / 25MHz

When programming the tick timer for periodic interrupt, the counter should be cleared to zero by software and then enabled. If the counter does not initially start at zero, the time to the first interrupt may be longer or shorter than expected.

Table 3-11 Tick Timer Counter Register

Offset: 0x18, 0x28, 0x38, 0x48			
Bit	**Description**	**Default**	**Access**
0:31	Tick Timer Counter	32'h00000000	LBC:r/w

When enabled, the tick timer counter registers increments every microsecond. Software may read or write the counter at any time.

3.2.7 RTM GPIO Register

The GPIO register for MVME8100 controls the four GPIO pins routed to the P0 and P2 connectors for use as general purpose IO signals on the RTM. Where as, only two GPIO for MVME8110 routed to the P2. Each GPIO signal has a weak pull down.

Table 3-12 RTM GPIO Register

Offset: 0x60			
Bit	**Description**	**Default**	**Access**
0:11	Reserved	12'h000	LBC:r
12:15	Current state of GPIO (3:0)	4'bxxxx	LBC:r
16:19	Reserved.	4'b0000	LBC:r
20:23	Set GPIO direction 0: input 1: output	4'b0000	LBC:r/w
24:27	Reserved	4'b0000	LBC:r
28:31	GPIO output value (if programmed as an output)	4'b0000	LBC:r/w

3.2.8 Scratch Register

Table 3-13 Scratch Register

Offset: 0x80			
Bit	**Description**	**Default**	**Access**
0:31	The Sticky Scratch Register (SSCR) is a 4-byte register that is intended for the programmer's use as a scratch pad and reset only by power cycle.	0	LBC:r/w

4.1 Overview

This chapter provides programming information for MVME8100/MVME8105/MVME8110 boards.

4.2 Interrupt Controller Assignments

The following table shows the external interrupts connected to the P5020/P5010 processors.

Table 4-1 P5020 External Interrupt Assignments

P5020 Interrupt	Interrupt Source	Description
IRQ0	None	Reserved
IRQ1	BCM5482 INT1	BCM5482 PHY interrupt 1 from LED_P1[2] pin
IRQ2	BCM5482 INT2	BCM5482 PHY interrupt 2 from LED_P2[2] pin
IRQ3/GPIO21	QUART_IRQ0	Quart Interrupt INTA
IRQ4/GPIO22	QUART_IRQ1	Quart Interrupt INTB
IRQ5/GPIO23	QUART_IRQ2	Quart Interrupt INTC
IRQ6/GPIO24	QUART_IRQ3	Quart Interrupt INTD
IRQ7/GPIO25	CPLD_TEMP_INT_L	Board Temperature interrupt (routed through CPLD)
IRQ8/GPIO26	CPLD_TIMER_INT_L	CPLD internal timers and Abort IRQ
IRQ9/GPIO27	BCM54616S INT	BCM54616S PHY interrupt from LED4 pin.
IRQ10/GPIO28	SRIO_IRQ_INT_L (only for MVME8100)	80HCPS1616 SRIO IRQ_N pin
IRQ11/GPIO29	RTC_INT_L	RTC interrupt

4.3 Ethernet PHY Management Addresses

There are total of three Ethernet PHYs on the MVME8100/MVME8105/MVME8110 boards which are managed through the P5020/P5010 dTSEC management interface. The following table shows the Ethernet PHY addresses.

Table 4-2 GbE PHY Address

MVME81XX GbE Port	PHY	PHY Address (PHYA 4:0)
Front Panel ETH	BCM5482 Port 1	00001
RTM GIGE4	BCM5482 Port 2	00010
RTM GIGE3	BCM54616S	00011
Note: For MVME8105, RTM GIGE4 is GENET2 and Front Panel ETH is GENET1.		

4.4 Local Bus Controller Chip select Assignment

The following table shows the devices connected to the P5020/P5010 LBC bus chip select.

Table 4-3 LBC Chip Select Assignment

LBC Chip Select	Local Bus Function	Size	Data Bus Width
0	MRAM	512KB	16-bits
1	QUART A	64KB	8-bits
2	QUART B	64KB	8-bits
3	QUART C	64KB	8-bits
4	QUART D	64KB	8-bits
5	CPLD	64KB	32-bits
6	Unused	-----	-----
7	Unused	-----	-----

4.5 I²C Devices

The following table shows the P5020 I²C busses and device addresses.

Table 4-4 I²C Busses and Devices

P5020 I²C Controller	I²C Device	I²C 7-bit (8-bit) Base Address	Device Type
1	SPD	0x50(0xA0)	AT24C02 (256x8)
1	User EEPROM	0x52(0xA4)	AT24C512 (65536 x 8)
1	VPD EEPROM	0x54(0xA8)	AT24C64 (8192x8)
1	RTM	0x57(0xAC)	Reserved for RTM
1	RTC	0x68(0xD0)	DS1337 real-time clock
1	PCIe Clock Generator	0x6E(0xDC)	IDT ICS9FG108 (default clock configuration is set by strapping resistors)
1	Outlet Temperature Sensor	0x48(0x90)	TMP112A
1	Inlet Temperature and CPU Temperature Sensor	0x4C(0x98)	ADT7461
2	Not Used		
3	Not Used		
4	XMC 1	0x50(0xA0)	XMC dependent
4	XMC 2	0x52(0xA4)	XMC dependent
4	SRIO (only for MVME8100) Switch Alternate Configuration EEPROM1	0x54(0xA8)	AT24C64D
4	SRIO (only for MVME8100) Switch Primary Configuration EEPROM1	0x55(0xAA)	AT24C64D
4	SRIO (only for MVME8100) Switch I²C Slave Interface	0x5D(0xBA)	80HCPS1616

Table 4-4 I²C Busses and Devices (continued)

P5020 I²C Controller	I²C Device	I²C 7-bit (8-bit) Base Address	Device Type
4	PCIe Switch SMbus	0x74(0xE8)	89H32NT24A
4	PCIe Clock Generator	0x6E(0xDC)	9FG104 (default clock configuration is set by strapping resistors)

Selection of Primary and Alternate Configuration EEPROM is determined by PCIe/SRIO (only for MVME8100) Root Complex/Endpoint switch S4-2. For more information, refer to the *S4 Switch section in the MVME8100/MVME8105/MVME8110 Installation and Use Manual*.

5.1 Overview

The MVME8100/MVME8105/MVME8110 boards use Das U-Boot, a boot loader software based on the GNU Public License. It boots the board and is the first software to be executed after the system is powered on.

Its main functions are:

- Initialize the hardware
- Pass boot parameters to the Linux kernel
- Start the Linux kernel
- Update Linux kernel and U-Boot images

This section describes U-Boot features and procedures that are specific to the MVME8100/MVME8105/MVME8110. For general information on U-Boot, refer http://www.denx.de/wiki/U-Boot/.

5.2 Accessing U-Boot

1. Connect the board to a computer with a serial interface connector and a terminal emulation software running on it. The serial connector of the board is found on the face plate.
2. Configure the terminal software to use the access parameters that are specified in U-Boot. By default, the access parameters are as follows:
   - Baud rate: 9600
   - PC ANSI
   - Eight data bits
   - No parity
   - One stop bit

These serial access parameters are the default values. These can be changed from within the U-Boot. For details, refer to the U-Boot documentation.

3. Boot the MVME8100/MVME8105/MVME8110

4. When prompted, press the **<Ctrl>+<C>** key.
   U-Boot aborts the boot sequence and enters into a command line interface mode.

Enter the command `setenv bootdelay -1; saveenv` to disable the U-Boot auto-boot feature and let the U-Boot directly enter the command line interface after the next reboot/power up.

5.3 Boot Options

5.3.1 Booting from a Network

In this mode, U-Boot downloads and boots the Linux kernel from an external TFTP server and mounts a root file system located on a network server.

1. Make sure that the following are accessible to the board from the TFTP server:
   ```
   kernel
   dtb
   ramdisk
   ```
2. Configure U-Boot environment variables:
   ```
   setenv ipaddr <IP address of the Board>
   setenv serverip <IP address of TFTP server>
   setenv gatewayip <gateway IP>
   setenv netmask <netmask>
   setenv bootargs 'root=/dev/ram rw console=ttyS0,9600n8
   ramdisk_size=700000 cache-sram-size=0x10000'
   saveenv
   ```
3. Transfer the files through the TFTP from the server to the local memory.
   ```
   tftpboot 1000000 kernel_image>
   tftpboot 2000000 <ramdisk>
   tftpboot F00000 <kernel dtb>
   ```
4. Boot the Linux from the memory.
   ```
   bootm 1000000 2000000 f00000
   ```

5.3.2 Booting from an Optional SATA Drive

1. Make sure that the following are saved in the SATA drive with ext2 partition:
   ```
   kernel
   dtb
   ramdisk
   ```
2. Configure U-Boot environment variable:
   ```
   setenv bootfile <kernel_image>
   setenv dtbfile <kernel dtb>
   setenv ramdiskfile <ramdisk>
   saveenv
   ```
3. Copy the files from the SATA drive to the memory:
   ```
   # option: scsi - interface, 0:1 - device 0 partition 1
   ext2load scsi 0:1 1000000 $bootfile
   ext2load scsi 0:1 2000000 $ramdiskfile
   ext2load scsi 0:1 f00000 $dtbfile
   ```
4. Boot the Linux in memory.
   ```
   bootm 1000000 2000000 f00000
   ```

5.3.3 Booting from a USB Drive

1. Make sure that the following are saved in the USB drive with FAT partition:
   ```
   kernel
   dtb
   ramdisk
   ```
2. Configure the U-Boot environment variable:
   ```
   setenv bootfile <kernel_image>
   setenv dtbfile <kernel dtb>
   setenv ramdiskfile <ramdisk>
   saveenv
   ```
3. Initialize USB drive:
   ```
   usb reset (’USB reset 1’ for RTM USB)
   ```

4. Load the files from the USB drive to the memory:
```
# option: usb - interface, 0:1 - device 0 partition 1
fatload usb 0:1 1000000 $bootfile
fatload usb 0:1 2000000 $ramdiskfile
fatload usb 0:1 f00000 $dtbfile
```
5. Boot the Linux in memory:
```
bootm 1000000 2000000 f00000
```

5.3.4 Booting from MMC

1. Make sure that the following are saved in the on-board eMMC device with FAT partition:
```
kernel
dtb
ramdisk
```
2. Configure the U-Boot environment variable:
```
setenv bootfile <kernel_image>
setenv dtbfile <kernel dtb>
setenv ramdiskfile <ramdisk>
saveenv
```
3. Initialize SD card:
```
mmcinfo
```
4. Load the files from the SD card to the memory:
```
# option: mmc - interface, 0:1 - device 0 partition 1
fatload mmc 0:1 1000000 $bootfile
fatload mmc 0:1 2000000 $ramdiskfile
fatload mmc 0:1 f00000 $dtbfile
```
5. Boot the Linux in memory:
```
bootm 1000000 2000000 f00000
```

5.3.5 Booting VxWorks Through the Network

In this mode, the U-Boot downloads and boots VxWorks from an external TFTP server.

1. Make sure that the VxWorks image is accessible by the board from the TFTP server.

2. Configure U-Boot environment variables:

```
setenv ipaddr <IP address of the Board>
setenv serverip <IP address of TFTP server>
setenv gatewayip <gateway IP>
setenv netmask <netmask>
setenv vxboot 'tftpboot $vxbootfile && setenv bootargs
$vxbootargs && bootvx'
setenv vxbootfile <VxWorks_image>
setenv vxbootargs 'dtsec(3,0)<IP address of TFTP server>:VxWorks
h=<IP address of TFTP server> e=<IP address of MVME8100>:ffffff00
b=<backplane IP> u=vxworks pw=vxworks f=0x80'
saveenv
```

For more information on bootline configuration/usage, refer to the *VxWorks Kernel Programmer's Guide*.

3. TFTP the files from the server to local memory, then boot:

```
run vxboot
```

5.4 MVME8100/MVME8105/MVME8110 Specific U-Boot Commands

Table 5-1 MVME8100/MVME8105/MVME8110 Specific U-Boot Commands

Command	Description
`base`	Print or set address offset
`bdinfo`	Print board info structure
`boot`	Boot default, i.e., run 'bootcmd'
`bootd`	Boot default, i.e., run 'bootcmd'
`bootelf`	Boot from an ELF image in memory
`bootm`	Boot application image from memory
`bootp`	Boot image through network using BOOTP/TFTP protocol
`bootvx`	Boot VxWorks from an ELF image
`cmp`	Memory compare
`coninfo`	Print console devices and information

Table 5-1 MVME8100/MVME8105/MVME8110 Specific U-Boot Commands (continued)

Command	Description
cp	Memory copy
cpu	Multiprocessor CPU boot manipulation and release
crc32	Checksum calculation
date	Get/set/reset date & time
dhcp	Boot image via network using DHCP/TFTP protocol
diags	Runs POST diags
dtt	Read temperature from digital thermometer
echo	Echo args to console
editenv	Edit environment variable
env	Environment handling commands
errata	Report errata workarounds
exit	Exit script
ext2load	Load binary file from a Ext2 file system
ext2ls	List files in a directory (default /)
false	Do nothing unsuccessfully
fatinfo	Print information about file system
fatload	Load binary file from a DOS file system
fatls	List files in a directory (default /)
fdt	Flattened device tree utility commands
go	Start application at address 'addr'
help	Print online help
i2c	I2C sub-system
iminfo	Print header information for application image
imxtract	Extract a part of a multi-image
interrupts	Enable or disable interrupts
itest	Return true/false on integer compare
loadb	Load binary file over serial line (kermit mode)

Table 5-1 MVME8100/MVME8105/MVME8110 Specific U-Boot Commands (continued)

Command	Description
`loads`	Load S-Record file over serial line
`loady`	Load binary file over serial line (ymodem mode)
`loop`	Infinite loop on address range
`mac`	Display and program the system ID and MAC addresses
`mapin`	Setup window to specified 36bit physical address
`md`	Memory display
`mii`	MII utility commands
`mm`	Memory modify (auto-incrementing address)
`mmc`	MMC sub system
`mmcinfo`	Display MMC info
`mtest`	Simple RAM read/write test
`mw`	Memory write (fill)
`nfs`	Boot image through network using NFS protocol
`nm`	Memory modify (constant address)
`pci`	List and access PCI Configuration Space
`ping`	Send ICMP ECHO_REQUEST to network host
`printenv`	Print environment variables
`reset`	Perform RESET of the CPU
`run`	Run commands in an environment variable
`saveenv`	Save environment variables to persistent storage
`scsi`	SCSI sub-system
`scsiboot`	Boot from SCSI device
`setenv`	Set environment variables
`setexpr`	Set environment variable as the result of eval expression
`sf`	SPI flash sub-system
`showvar`	Print local hushshell variables
`sleep`	Delay execution for some time

Table 5-1 MVME8100/MVME8105/MVME8110 Specific U-Boot Commands (continued)

Command	Description
`source`	Run script from memory
`test`	Minimal test like /bin/sh
`tftpboot`	Boot image through network using TFTP protocol
`tsi148`	Initialize and configure Tundra Tsi148
`usb`	USB sub-system
`usbboot`	Boot from USB device
`version`	Print monitor version

5.5 Updating U-Boot

To update the U-Boot, place the image in the RAM (address 0x1000000 in this example) before copying it to the SPI flash.

The following procedure will replace the image in SPI bank 0:

1. Select SPI flash # 0:
   ```
   sf probe 0
   ```
2. Erase 0x90000 bytes starting at SPI address 0:
   ```
   sf erase 0 0x90000
   ```
3. Write 0x90000 bytes from RAM address 0x1000000 starting at SPI address 0:
   ```
   sf write 0x1000000 0 0x90000
   ```

To replace the image in SPI bank 1, replace Step 1 with Select SPI flash # 1:
```
sf probe 1
```

A.1 Artesyn Embedded Technologies Documentation

The publications listed below are referenced in this manual. You can obtain electronic copies of Artesyn Embedded Technologies publications by contacting your local Artesyn sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

Go to https://www.artesyn.com/computing/search/documents/.

Under **FILTER OPTIONS**, click the Document types drop-down list box to select the type of document you are looking for.

In the **Search** text box, type the product name and click **GO**.

Table A-1 Artesyn Embedded Technologies Publications

Document Title	Publication Number
MVME8100 Data Sheet	MVME8100-DS
MVME8105 Data Sheet	MVME8105-DS
MVME8110 Data Sheet	MVME8110-DS
MVME8100/MVME8105/MVME8110 Installation and Use	6806800P25
MVME8100/MVME8110 Quick Start Guide	6806800P26
MVME8100/MVME8110 Safety Notes Summary	6806800P27
MVME7100 Product Errata	6806800K31

A.2 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table A-2 Related Specifications

Organization and Standard	Document Title
VITA Standards Organization	
VME64	ANSI/VITA 1-1994
VME64 Extensions	ANSI/VITA 1.1-1997
2eSST Source Synchronous Transfer	ANSI/VITA 1.5-2003
Processor PMC	ANSI/VITA 32-2003
PCI-X for PMC and Processor PMC	ANSI/VITA 39-2003
XMC Switched Mezzanine Card Auxiliary Standard, September 2005	VITA 42.0-2005
XMC PCI Express Protocol Layer Standard, June 2006	VITA 42.3-2006
Conduction Cooled PMC	ANSI/VITA 20 - 2001
PMC I/O Module (PIM) Draft Standard	VITA 36 Draft Rev 0.1 July 19, 1999
Universal Serial Bus	
Universal Serial Bus Specification	Revision 2.0 April 27, 2000
PCI Special Interest Group	
PCI Local Bus Specification, Revision 2.2	PCI Rev 2.2 December 18, 1998
PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification, Revision 2.0a	PCI-X EM 2.0a August 22, 2003

Table A-2 Related Specifications (continued)

Organization and Standard	Document Title
PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a	PCI-X PT 2.0a July 22, 2003
Institute for Electrical and Electronics Engineers, Inc.	
IEEE Standard for a Common Mezzanine Card Family: CMC	IEEE1386 Oct 25, 2001
IEEE Standard Physical and Environmental Layer for PCI Mezzanine Cards: PMC	IEEE1386.1 Oct 25, 2001
Conduction cooled VME mechanics	IEEE 1101.2 - 1992
Additional Mechanical Specifications	IEEE 1101.10 - 1996
IEEE Standard for Mechanical Core Specifications for Microcomputers	IEEE 1101.1 - 1998

A.3 Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table A-3 Manufacturer's Publications

Document Title and Source	Publication Number
NXP Semiconductors	
P5020/P5010 QorIQ Integrated Processor Hardware Specifications	P5020EC
P5020 QorIQ Integrated Multicore Communication Processor Reference Manual	P5020RM
Integrated Device Technology	
IDT 89HPES32NT24xG2 PCI Express Switch User Manual	
CPS-1616 Central Packet Switch Datasheet	

NOTES

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